Low Loss Multi-Layer Wiring for Superconducting Microwave Devices

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Complex integrated circuits require multiple wiring layers. In complementary metal-oxide-semiconductor (CMOS) processing, these layers are robustly separated by amorphous dielectrics. These dielectrics would dominate energy loss in superconducting integrated circuits. Here we demonstrate a procedure that capitalizes on the structural benefits of inter-layer dielectrics during fabrication and mitigates the added loss. We separate and support multiple wiring layers throughout fabrication using SiO_2 scaffolding, then remove it post-fabrication. This technique is compatible with foundry level processing and the can be generalized to make many different forms of low-loss multi-layer wiring. We use this technique to create freestanding aluminum vacuum gap crossovers (airbridges). We characterize the added capacitive loss of these airbridges by connecting ground planes over microwave frequency $\lambda/4$ coplanar waveguide resonators and measuring resonator loss. We measure a low power resonator loss of $\sim 3.9 \times 10^{-8}$ per bridge, which is 100 times lower than dielectric supported bridges. We further characterize these airbridges as crossovers, control line jumpers, and as part of a coupling network in gmon and fluxmon qubits. We measure qubit characteristic lifetimes (T_1's) in excess of 30 μs in gmon devices.

Two dimensional superconducting qubit architectures will require multi-layer wiring.[1–3] Multiple wiring layers are used in standard integrated circuits to route signals past one another to individually address a two dimensional grid of elements. A basic form of multi-layer wiring is a dielectric crossover, whereby a mechanically stable layer of dielectric separates two metal layers. While these crossovers offer robust large scale control, the amorphous dielectrics typically used are quite lossy, with loss tangents $\tan\delta \approx 10^{-3}$.[4,5] We limit participation of similar dielectrics ($p_i < 10^{-3}$) to achieve state-of-the-art qubit quality factors ($Q_i > 1 \times 10^6$).[6,7] To maintain this level of qubit coherence while increasing circuit complexity many have turned to dielectric-free crossovers. These free standing metallic crossovers, known as airbridges, are widely used in low-loss microwave circuits[8,9] as well as superconducting circuits.[10,11] Airbridges are typically fabricated using re-flowed photoresist as a scaffold, which is removed immediately after birdge fabrication and prior to further processing. Previous works have characterized the fabrication process for aluminum airbridges, specifically focusing on mechanical stability and dielectric loss due to remnant photoresist.[12] Without dielectric support, the mechanical strength of freestanding airbridges relies on an arched shape. Airbridges with spans much larger than their arched height tend to bend under the pressure of resist spins and bakes. Thus, airbridges are made taller to span longer distances. Bridge height is limited by future processing, as standard high-resolution resists ($\sim$ 1-10 μm thick) fail to protect taller bridges from aggressive processing steps such as ion etching or lift-off. Additionally, released airbridges typically cannot withstand the sonication widely used to remove surface contaminants. To avoid these problems, we fabricate airbridges last during qubit production. This solution limits processing and is cumbersome. The extended high temperature bakes required to re-flow the resist scaffold alters Josephson Junction resistances.

Here we describe different type of airbridge crossover that is scaffolded by a $\sim$ 1 μm thick silicon oxide (SiO_2) dielectric layer. This layer supports the bridges until release in the final step of fabrication using low temperature anhydrous hydrofluoric acid vapor (VHF). We show this VHF is compatible with standard qubit materials (including Aluminum and AlOx Josephson Junctions). During the fabrication, the SiO_2 scaffolding stabilizes these bridges through aggressive sonication and resist coating, thus decoupling the bridges span from it's height. Mechanical tests indicate these bridges span distances of at least 70 μm reliably. The added capacitive loss per bridge is comparable to photoresist scaffolded airbridges and is $\sim 100\times$ less lossy than conventional dielectric crossovers. Furthermore, these dielectric scaffolded airbridges are compatible with more standard CMOS processing, and provide an avenue toward scalable control wiring for a two dimensional grid of qubits.

We fabricate these bridges after defining aluminum basewiring on high resistivity (>10 kΩ·cm) intrinsic (100) plane silicon substrates. We optically pattern a trilayer[13] stack of resist as a lift-off mask and electron beam (e-beam) deposit 1 μm of SiO_2 to define the SiO_2 scaffold. We use a similar lift-off process to define the bridge itself, except prior to deposition, we use an in-situ 400 V, 0.8 mA/cm^2 argon ion mill to remove the exposed native aluminum oxide on the basewire. This mill allows DC electrical contact between base-wire aluminum and the 600 nm thick airbridge aluminum. After all further processing we use a dry VHF etcher (PRIMAXX ®VHF Etch Release Technology) to release the bridges by removing the scaffolding SiO_2. The chamber is pumped

low vacuum, and the die is heated to 45 Celcius on a 3 inch silicon carrier wafer. A mixture of HF vapor, nitrogen, and ethanol is then bled into the chamber at a total pressure of 125 Torr (parameters in Table I). The scaffold SiO_2 and native oxide of the exposed silicon substrate are removed after 2 cycles of 15 seconds without breaking vacuum, as shown in Fig 1(c). Vapor phase release significantly reduces the mechanical strength required to overcome sticition, a common failure in microelectromechanical systems (MEMs) devices.[14,15] This process does not attack other materials used in qubit fabrication including aluminum, aluminum oxide, and silicon.

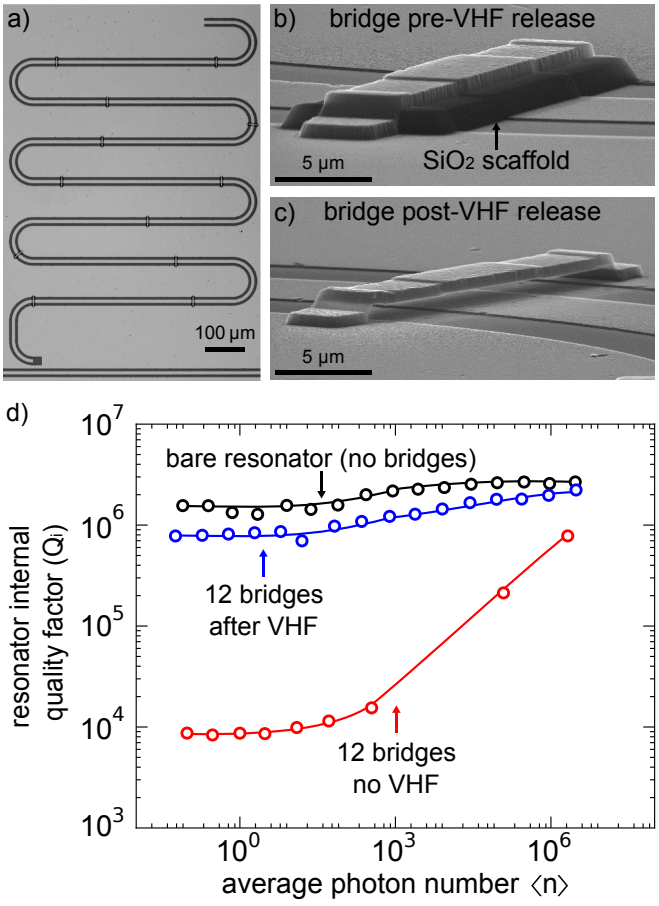

Figure 1. (a) Optical micrograph of a CPW $\lambda/4$ resonator with 12 crossovers over the center trace capacitively coupled to a feed-line. (b) Crossover spanning the resonator before removing SiO_2 scaffold. (c) Freestanding airbridge crossover after VHF treatment. (d) Representative resonator Q_i vs average photon excitation. Leaving the SiO_2 under bridges greatly reduces the resonator's quality, as would most deposited dielectrics. After removing the SiO_2 the resonator's quality recovers to about a factor of two lower than bare witness resonators. The twelve evenly spaced bridges only cover $\sim 0.7\%$ of the $\lambda/4$ resonator geometry. Resonators without bridges (bare resonators) show no substantial difference in quality with or without VHF treatment.

In our superconducting circuits these airbridges serve two main functions: 'jumper airbridges' which hop lines over each other and 'ground plane airbridges' which connect ground planes over lines. Jumper airbridges hop circuit elements over each other for stronger couplings, smaller footprints, and design flexibility. These SiO_2 scaffolded airbridges can be made with contact pads as small as 1 μm^2 and allow even micron width lines to hop over each other. Ground plane airbridges are commonly used to electrically connect ground planes to suppress parasitic microwave frequency slot line modes which modify couplings and act as qubit loss channels in coplanar waveguide (CPW) geometries.[16,17] These airbridges also route return currents to reduce unwanted cross-talk between control lines.

VHF Flow (SCCM)	N_2 Flow (SCCM)	Ethanol Flow (SCCM)
190	1425	210

Table I. VHF etch parameters.

We measure the added capacitive loss from airbridges using $\lambda/4$ CPW resonators. To measure resonator loss, we cool down chips in a heavily filtered[18] adiabatic demagnetization refrigerator with a base temperature of 50 mK. We extract resonator internal quality factor (loss $= 1/Q_i$) by measuring and fitting the microwave scattering parameters versus frequency near resonance.[19] Each chip has ten resonators capacitively coupled (Q_c between5×10^5 and 1×10^6) to a common feedline. These resonators have between zero and ninty-eight ground-plane airbridges spanning their center trace. The airbridges are 3 μm wide and have a height above the center trace set by the original dielectric thickness of 1 μm. In Fig. 1(a) we show one such resonator resonator spanned by 12 ground plane airbridges equally spaced along the resonator after the coupling arm. All resonators have a 10 μm center trace and a 5 μm gap to ground on either side, and resonance frequencies near 6 GHz.

We compare loss between three styles of resonators: resonators spanned by scaffolded bridges (Fig. 1(b)), resonators spanned by airbridges (after VHF release, Fig. 1(c)), and the on-chip resonators with no bridges. In Fig. 1(d) we display internal quality factor data for these three resonators. For clarity, we show only a single representative trace from each. The single photon loss limit approximately captures the physics of energy loss in superconducting qubits at the same frequency. The bare witness resonator (with no crossovers) has a low power internal quality factor of around 1.5×10^6 which is consistent with single layer fabrication resonators of the same geometry. We saw little to no difference in bare resonator quality factors between chips with or without the VHF process. When the SiO_2 is left intact, (as it would be in typical dielectric crossovers) the low power Q_i drops to around 1×10^4. This is consistent with an amorphous SiO_2 loss tangent of $\tan\delta \approx 10^{-3}$ and a participation of 10% (roughly the added capacitance for twelve bridges). After the VHF treatment, the Q_i of resonators with twelve bridges recovers to a factor of 2 lower than

the bare resonators. We measure the scaling of this residual loss with number of bridges between zero and ninty-eight. The internal quality factor decreases with increasing number of bridges and lines of best fit indicate added loss at low power of 3.9×10^{-8} per bridge.[13]

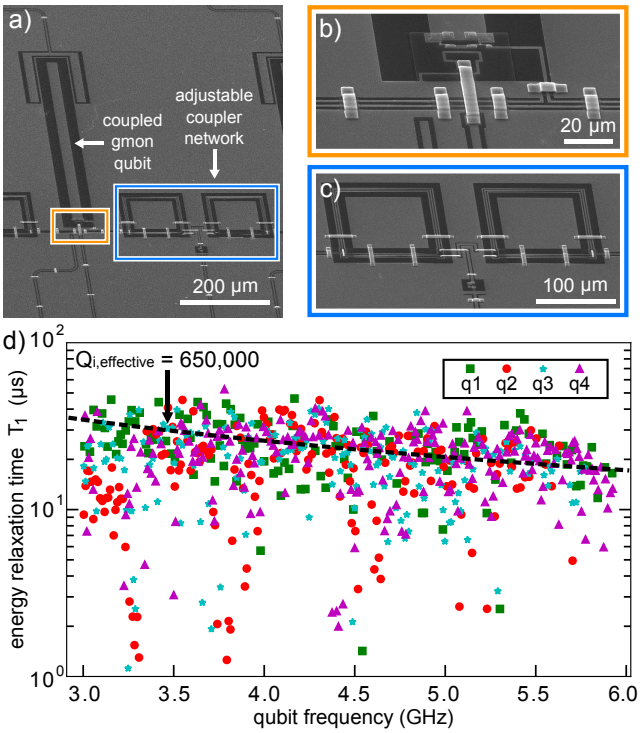

Figure 2. (a) Scanning electron microscope image of a gmon qubit and it's neighboring adjustable coupler network. (b) Airbridges are used in the coupler to both connect lines (hopping over ground plane) and shield lines (hoping over coupler and qubit inductor lines) (c) Airbridges are also used to hop the flux bias line over the qubit inductor lines. (d) Qubit T_1 measurements from four different gmon qubits, with an average around 20 μs.

We use these low-loss airbridges as an integral part of gmon qubits. These qubits are transmon qubits[20] with inductive taps placed between DC SQUID and ground plane to allow adjustable coupling to nearest neighbors.[21] It is critical that any added loss from the airbridges does not compromise the qubit coherence. In Fig. 2(a) we display one such gmon qubit with its neighboring coupler network. We bias these qubits' DC SQUID loop with maximum DC current of 2 mA. This current flows entirely through a jumper crossover in-line with the flux bias line (Fig. 2(b)) and shows no evidence of on-chip heating. In the qubit circuit, we use many ground plane airbridges as well as a set of jumper airbridges in-line with the coupler's geometric inductor (Fig. 2(c)). This jumper airbridge allows a gradiometric turn which further reduces crosstalk. These jumper airbridges are only 1.5 μm wide, highlighting their small footprint. It is also important to note that these bridges are fabricated prior to Josephson junction deposition, and are robust after all of the further processing, with yield limited by lithography errors. In Fig. 2(d) we show qubit energy relaxation time (T_1) spectra over 3 GHz of tunable qubit frequency for four different qubits. The spectrum is well represented by a constant effective $Q_i \approx 6.5\times10^5$, with small sections where the T_1 drops dramatically. These spectra are consistent with qubit loss dominated by dielectric surface loss from the SQUID area.[6] The bridges themselves do not appear to greatly impact the qubit T_1 spectra.[13]

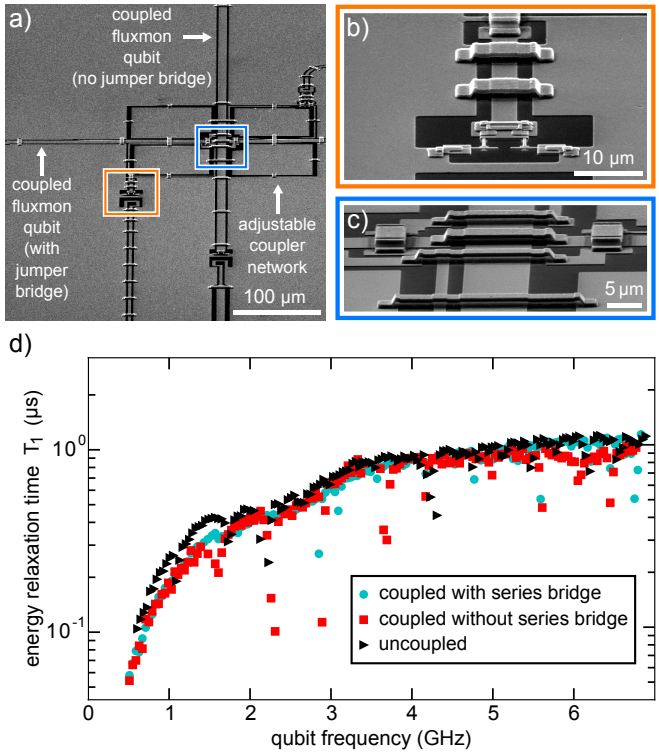

Figure 3. (a) Scanning electron microscope image of two coupled fluxmon qubits and their adjustable coupler. (b) Image of ground plane and jumper airbridges near the coupler DC SQUID loop. (c) Image of a network of bridges with SiO_2 scaffolding removed after VHF processing. (d) Qubit T_1 measurements from three different fluxmon qubits. We see no systematic difference between coupled with series bridge, coupled with no series bridge, and uncoupled, indicating bridges do not impact the coherence.

We also use these airbridges as integral parts of our fluxmon[22] flux qubit circuits, for both isolated and coupled qubits. The main inductance and capacitance of the fluxmon is distributed over a long CPW segment that is terminated with an electrical short to ground at one end and a DC SQUID shorted to ground at the other. We use both ground plane airbridges over the qubit's CPW and jumper airbridges in-line with the qubit's CPW and the couplers as well. We tested three variations of fluxmon qubits on the same chip: uncoupled, coupled with jumper bridge, and coupled without jumper bridge. The uncoupled qubits only use ground plane airbridges. For the coupled qubits, the CPW center trace of one qubit

jumps over the CPW center trace of the other qubit via an airbridge, as shown in Fig. 3(a), while the other qubit does not have any in-line jumper airbridges.

The resulting qubit T_1 vs. frequency at symmetric bias (zero tilt bias) is shown in Fig. 3(d) for the three qubit variations. The background dissipation is believed to come from $1/f$ flux noise at low frequencies[22,23] extrinsic to the airbridges, with some other inductive loss extrinsic to the airbridges dominating at high frequencies. We find no measurable difference in coherence between the two types of coupled qubits. This is consistent with a very high quality galvanic contact between the jumper bridge and the qubit's CPW. Furthermore, we see no measurable difference in coherence between the coupled and uncoupled qubits, despite the fact that the coupled qubits are in very close proximity to a coupler circuit (the thin traces and ground plane pads in Fig. 3(c)) containing many crucial jumper and ground plane airbridges. This retained coherence is very important for scaling up fluxmon circuits with many jumper crossovers and couplers, in order to couple one qubit to many others at once for quantum annealing applications.

In summary, we have demonstrated a procedure that utilizes the structural benefits of inter-layer dielectrics for multi-layer wiring, while mitigating the capacitive loss. We rigidly scaffold top wiring layers with amorphous SiO_2 through subsequent fabrication steps, then use VHF to remove the dielectric in the final step of device fabrication. We use this process to fabricated low loss airbridges that are robust against strong sonication and other aggressive fabrication steps, and have a low profile. We measure the added loss per ground plane bridge over resonators to be $\sim 3.9 \times 10^{-8}$ at low power. We have demonstrated these bridges use in different superconducting qubit devices and measured little to no effect on the coherence of the qubits. By replacing the lift-off steps in the bridge fabrication with more standard blanket depositions and via etches, this process is completely compatible with standard multi-layer CMOS processing. This process also generalizes to multiple wiring layers as the process could be repeated to stack more bridges on each other to allow even more complex wiring.

I. ACKNOWLEDGMENTS

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Supplementary Material for "Low Loss Multi-Layer Wiring for Superconducting Microwave Devices"

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We provide supplementary data and calculations.

I. RESONATOR LOSS PER BRIDGE

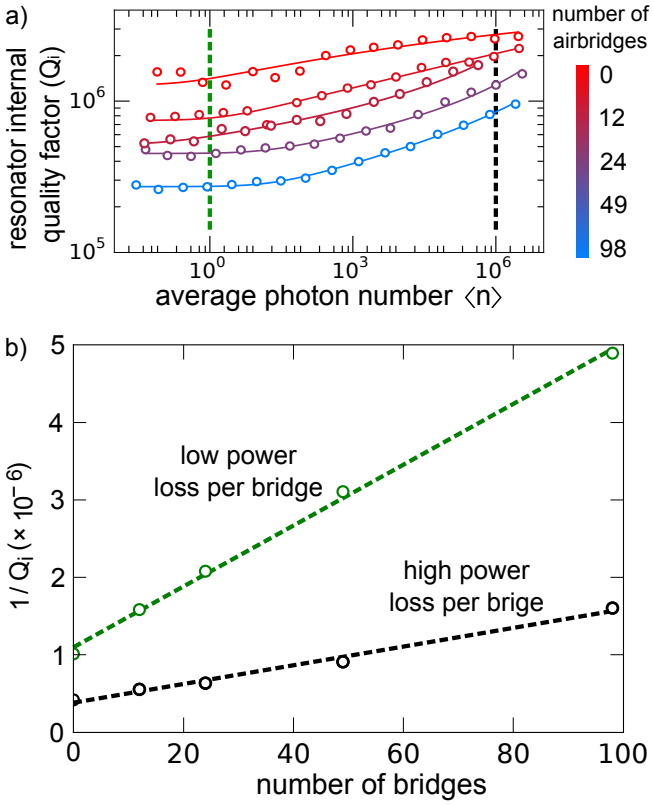

Figure 1. Resonator loss ($1/Q_i$) cuts at low power (average photon population of $\sim 10^0$) and high power (average photon population of $\sim 10^6$) plotted against number of bridges. Lines of best fit give and 3.9×10^{-8} (1.2×10^{-8}) loss per bridge at low (high) power.

We design $\lambda/4$ coplanar waveguide (CPW) resonators with a variable number of ground plane airbridges to measure the added capacitive loss per bridge. We use the the anhydrous hydrofluoric acid vapor (VHF) process detailed in the main paper to remove the SiO_2 scaffold prior to cooling down these resonators. We measure the scaling of the resonator loss with between 0 and 98 bridges spanning the center trace. In Fig. 1 (a) we display representative Q_i vs average photon excitation for these resonators. The resonator internal quality factor decreases with increasing number of bridges. In Fig. 1 (b) we show cuts of loss ($1/Q_i$) vs number of bridges at low and high power. A line of best fit indicates an added loss at low power of $1.2{\times}10^{-7}$ per fF of added capacitance, or $3.9{\times}10^{-8}$ per bridge at low power. This is a factor of two higher loss per added capacitance of photoresist scaffolded airbridges (5.08×10^{-8} per fF).[1] It is also important to note that if either of these bridges were coupled to a lumped capacitor, they would display a factor of two more loss. Here we are protected from the full loss by the cosine voltage profile along the $\lambda/4$ resonator.

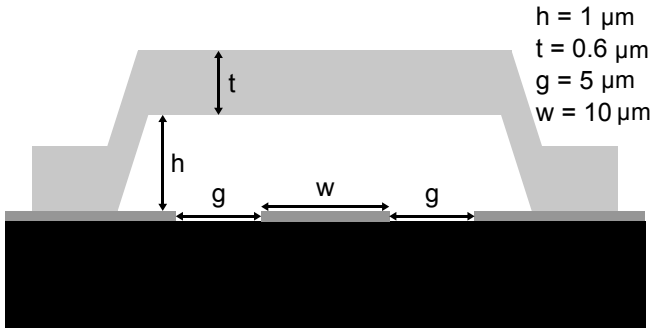

Figure 2. CPW dimensions of aluminum resonators on a silicon substrate. The width of the bridge in into the page is $l = 3$ μm.

Here we calculate the expected added low-power loss per bridge:

$$1/Q_{i,bridge} = \tan\delta \times p_{loss}$$

$$\approx \tan\delta \left(\frac{2t_{loss}}{h}\right)\left(\frac{1}{\epsilon_{r,loss}}\right)\left(\frac{C_{bridge}}{C_{\lambda/4}}\right)$$

$$= 1 \times 10^{-9} \ \frac{\text{loss}}{\text{nm}} \left(\frac{t_{loss}}{\epsilon_{r,loss}}\right)$$

Where the factor of 2 assumes that the lossy material is on both the top of the center conductor and bottom

Resist Type	Hot Plate Bake Temperature (C)	Bake Time (minutes)	Approximate Thickness (nm)	Vertical Oxygen Barrel Ash Rate[a] (nm/sec)	Vertical Oxygen Ash Rate in ICP[b] (nm/sec)
PMMA	160	10	240	2.10	0.92
PMGI					
SF5 (etch)	160	5	200	NA	NA
SF11 (liftoff)	160	5	1300	NA	NA
SPR (955-0.9)	90	1.5	900	0.71	0.40

[a] 0.3 torr O_2, 100 watts RF bias power
[b] 0.015 torr O_2, 100 watts ion power, 0 watts RF bias power

Table I. Parameters for resists used in tri-layer stack. All resists are spun on at 1500 rpm for 45 seconds. SF5 is used for etch processes while the thicker SF11 is used for liftoff processes. We use a 0.4 second exposure at ∼420 mW/cm^2 at the wafer to expose the SPR, and do a post exposure bake on a 110 C hot plate for 90 seconds to improve resist contrast and development stability. Etch rates measured with blanket films of the corresponding resist types.

of the bridge equally. We also assumed a loss tangent of 1×10^{-3}, consistent with previous works.[2,3]. The capacitances are calculated as follows:

$$C_{\lambda/4} = \frac{1}{8 f_0 Z_0} \approx 470 \text{ fF}$$

$$C_{bridge} = \epsilon_0 \left(\frac{\mathrm{w} l}{\mathrm{h}} \right) \approx 0.266 \text{ fF}$$

Where we assume the geometries are all as displayed in figure 2. If we then assume the loss comes from the native oxide of aluminum, $t_{loss} = 3$ nm and $\epsilon_{loss} = 10$, we get 3×10^{-10} loss per bridge. This greatly under predicts the loss. If we assume it is left over SiO_2 ($\epsilon_{loss} = 4$) it would require around 100 nm of lossy material to recover the above measured loss per bridge in this simple parallel plate model. We do not see this thickness of residue in edge on SEMs similar to those in the main paper.

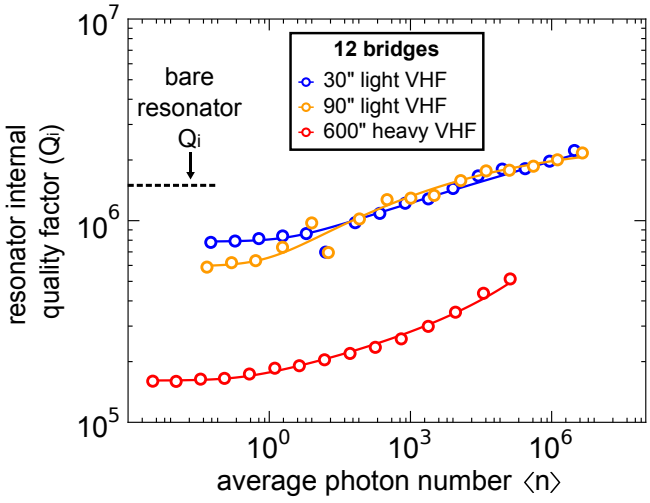

Figure 3. Representative resonator Q_i measurements for differing amounts of VHF treatment. The bare resonator has no bridges, but did receive 30 seconds of the light VHF treatment detailed in the main paper.

II. EFFECT OF OVER-ETCHING SiO_2

The etch rate of the SiO_2 in VHF will depend on the amount of SiO_2 present. This loading effect could lead to remnant SiO_2 and therefore increased loss. Over-etching may also lead to excess loss, as VHF is known to leave residue from condensation under certain etch conditions.[4] We cooled down resonators etched for longer in VHF, as well as resonators with a much more substantial VHF etch (parameters in Tab. II), to test the effects of over-etching.

VHF Flow (SCCM)	N_2 Flow (SCCM)	Ethanol Flow (SCCM)
880	325	720

Table II. Heavy VHF etch parameters.

In Fig. 3 we plot Q_i vs average photon population in resonators that underwent the above processes. We note that there is a very small effect on the internal quality from over etching for up to 3 times the length required to remove the SiO_2 (this variation in Q_i is expected for device-to-device variation). However, when we use the stronger etch parameters for a much longer time, resonator's internal quality factor drops to around 2×10^5.

III. FULL FABRICATION

The basewire deposition, lithography, and wet-etch (using Tetramethylammonium hydroxide (TMAH) based photo resist developer) are covered in detail in a previous publication.[5] We use this tri-layer stack of resist, consisting of PMMA (Polymethylmethacrylate 4% in Anisole), SF series PMGI, and i-line positive photoresist (SPR 955-0.9) to protect the aluminum from developer etching during dry etch and lift-off steps (Tab. I). The top resist layer is a standard photoresist for defining features ~ 1 μm in critical dimension. The middle layer of resist

allows for variable undercutting for reliable lift-off and and etching profiles. The bottom layer of resist is used to protect the aluminum layer during photo resist development, and is known to etch readily in oxygen plasmas.[6,7] We use a GCA Auto-Stepper 200 to expose optical patterns. The topmost resist layer develops where exposed. The PMGI develops without being exposed, undercutting the SPR (Fig. 4 a-b). The PMMA is not etched by the TMAH based developer and thus protects the aluminum from being etched. We then oxygen ash the PMMA to remove it where exposed and slightly undercut the SPR (Fig. 4 c).

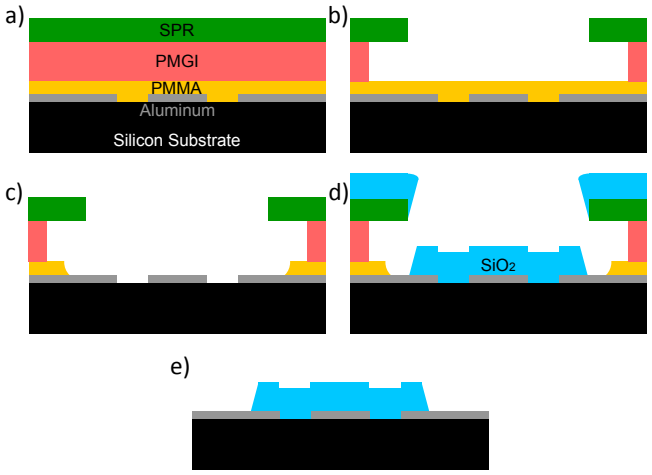

Figure 4. Example tri-layer lift-off process step through. (a) Cartoon profile of tri-layer stack of resists top-to-bottom SPR 955, PMGI, PMMA, then an etched 100 nm aluminum film on an intrinsic silicon substrate (not to scale). (b) After photo lithography we develop to remove SPR where exposed and the PMGI develops isotropically at a rate of ∼2.4 μm/min. (c) The PMMA is nearly directionally ashed (due to RF bias and low pressures) in an oxygen plasma. (d) The SiO_2 is e-beam deposited in a high vacuum system. (e) The resist is stripped clean with the help of the undercut layers breaking up the lift-off film.

This tri-layer process is made compatible with both etching and lift-off processes by changing the PMGI thickness and PMMA ashing method. For etch steps, the oxygen ash is done prior to the aluminum etch in-situ in an inductive coupled plasma (ICP) tool (Panasonic E626I) with 15 mT of oxygen and 200 W plasma power with no RF bias onto the devices. For lift-off steps we ash the PMMA in a barrel asher (Technics PEII) with 300 mT of oxygen with 300 W of RF power. The middle PMGI layer also serves as a buffer between the solvents in the SPR and the PMMA. Direct contact between SPR and PMMA leads to variable intermixing and unstable PMMA ash rates. We use a thicker layer of PMGI SF11 (∼ 1.1 μm) to fabricate the SiO_2 scaffolded airbridges bridges. We do one round of lithography and ashing, then load into a high vacuum electron beam deposition tool (base pressure ∼ 1×10^{-6} Torr) and deposit 1 μm of silicon oxide (Fig. 4 d). The resist is stripped using an N-Methyl-2-pyrrolidone (NMP) based resist stripper lifting off the excess silicon oxide (Fig. 4 e), and a second round of spins and photo-lithography defines the top metal. We load into another electron beam deposition tool ($P_{base} = 2 \times 10^{-7}$ Torr), do an in-situ argon ion mill to remove the oxide of the exposed aluminum. We use a 400 V, 0.8 mA/cm^2 beam for 6 minutes with and continuous Argon flow of 3.6 sccm for this clean. We then deposit 600 nm of aluminum to form the bridge. We strip the resist as above to lift-off the excess metal.

We have greatly stabilized our lithography and processing by using this tri-layer stack of resists. Stripping resist after dry etch steps is more stable as all the resist in direct contact with the substrate and metal is shielded from the high energy ions needed to etch the aluminum oxide and subsequently the underlying aluminum. This allows solvents to get under hardened resist and reduces residues. This tri-layer of resist also greatly stabilizes lift-off processing. The undercut of the resist disconnects the lifted off film from the intended remnant material. This stack up also allows for an arbitrary number of lithography steps to be performed without worry of developer etching aluminum. This protection enables quick recovery from errors in lithography.

IV. GMON T_1 FREQUENCY DEPENDENCE

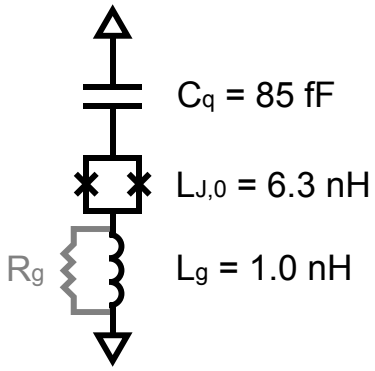

Figure 5. A simplified circuit of a lone gmon. The shaded resistor represents surface loss from the amorphous dielectrics near the thin geometric inductor lines.

All of the bridges in the gmon circuit are most strongly coupled to the qubit's geometric inductor. Therefore, additional loss from these bridges would mostly add to that of the stray capacitance of the geometric inductor. The coherence of the gmon qubit is protected from capacitive loss in it's thin inductor lines by a voltage divider between it's SQUID inductance ($L_{J,0} \approx 6.3$ nH) and the linear geometric inductance ($L_g \approx 1.0$ nH). We flux tune this SQUID inductance larger to decrease the qubit's frequency, thus the qubit energy relaxation time (T_1) would have a frequency dependence, as the ratio of SQUID to

geometric inductance changes. Here we calculate the expected frequency dependence of this loss. It is often easier to think about loss in terms of an effective quality factor (Q_i). For this channel:

$$Q_i = \frac{R_g}{Z_q}\left(\frac{V_q}{V_g}\right)^2 \tag{1}$$

Where $Z_q \approx (L_J/C_q)^{1/2}$ is the qubit impendance, R_g is the loss from surface amorphous dielectrics near the geometric inductor lines, V_q is the voltage drop across the qubit capacitor (C_q), and V_R is the voltage drop across the geometric inductor tail (L_g). We neglect the stray capacitance of the inductor tail as the qubit operates well below the resonance of the inductor circuit (~ 12 GHz), and instead consider it only as a source of loss. We can calculate V_g in terms of V_q using the voltage divider:

$$V_g = V_q\left(\frac{L_g}{L_J + L_g}\right) \approx V_q\left(\frac{L_g}{L_J}\right) \tag{2}$$

we can also define $\omega_q = 1/(L_J C_q)^{1/2}$ and thus:

$$Q_i \approx \frac{R_g}{C_q L_g^2}\left(\frac{1}{\omega_q}\right)^3 \tag{3}$$

and to convert to an energy relaxation limit $T_1 = Q_i/\omega_q$ of the qubit:

$$T_1 = \frac{R_g}{C_q L_g^2}\left(\frac{1}{\omega_q}\right)^4 \tag{4}$$

We do not witness this strong frequency dependence in the qubit's energy relaxation spectrum, indicating the qubit's coherence is not limited by this loss channel.

Another main loss channel for these qubits is due to surface dielectrics in the qubit capacitor. We fabricate witness resonators (etched at the same time as the qubit capacitor, but cooled down separately) to investigate this limit on qubit coherence. Witness resonators with a similar geometry have a much larger $Q_i \approx 3\times10^6$ indicating that the qubits' T_1 is not limited by the capacitor itself. Most likely the gmon's T_1 is limited by interfacial amorphous dielectrics near the Josephson junction electrodes.[5]

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