Blueprint for a microwave ion trap quantum computer

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A universal quantum computer will have fundamental impact on a vast number of research fields and technologies. Therefore an increasingly large scientific and industrial community is working towards the realization of such a device. A large scale quantum computer is best constructed using a modular approach. We present the blueprint for an ion trap based scalable quantum computer module which makes it possible to create an arbitrarily large quantum computer architecture powered by long-wavelength radiation. This quantum computer module controls all operations as a stand-alone unit, is constructed using silicon microfabrication techniques and within reach of current technology. To perform the required quantum computations, the module makes use of long-wavelength-radiation quantum gate technology and relies only on a vacuum environment and global laser and microwave fields. To scale this microwave quantum computer architecture beyond one module we also present a new approach that makes use of ion transport between different modules, thereby allowing connections between arbitrarily many modules for a large scale architecture. A high-error-threshold surface error correction code making use of such module interactions can be implemented in the proposed architecture to execute fault-tolerant quantum logic operations. With only minor adjustments these modules are also suitable for alternative ion trap quantum computer architectures, such as schemes using photonic interconnects.

INTRODUCTION

Trapped atomic ions are a very promising candidate for the realization of a universal quantum computer having demonstrated robust, high-fidelity state preparation [1, 2] and detection [1, 3], high-fidelity universal gate operations [1, 4, 5] and long qubit coherence times [6, 7].

Using ion transport with trap arrays to realize an ion trap quantum computer was proposed by Kielpinski et al. [8]. Developing a realistic quantum computing architecture with trapped ions has since attracted a lot of interest. Recently, a very exciting approach addressing this challenge was presented by Monroe et al. [9], where ion trap modules, also called elementary logic units (ELUs), are photonically interconnected using commercial fibres and optical crossconnect switches. This proposal demonstrates that going from one to many modules is within reach of current technology and thereby provides an interesting path to a large scale ion trap quantum computer. Theoretical investigations of this approach have shown that it can be used for fault-tolerant quantum computations [10] and that noisy and lossy links are sufficient for quantum computing, when combined with entanglement purification [11].

An important challenge towards building a large scale ion trap quantum computer still remains: the development of a detailed blueprint for a scalable module capable of performing all required fundamental quantum operations and acting as a stand-alone small scale quantum processor. The module must also offer efficient connections with additional modules to create a universal quantum computer architecture.

In previously proposed ion trap quantum computing architectures, modules are powered by laser-driven single and multi-qubit gates. However, vast amounts of individually controlled, stable laser beams required in such a concept would make the required engineering to build a large scale quantum computer quite challenging. Here we propose an architecture that is based on global long-wavelength radiation and locally applied magnetic fields. The gate interactions are based on a mechanism first proposed by Mintert and Wunderlich in 2001 [12] making use of magnetic field gradients within dedicated entanglement zones. Only global laser light sheets are required for loading, Doppler cooling and state preparation and detection of ions, while pairs of Raman laser beams that are used for laser driven quantum gates requiring careful alignment in each entanglement zone are not required in our approach. Architectures that rely on laser gates may require millions of individual pairs of beams that have to be precisely aligned with respect to each other and individual entanglement regions and need to be individually controlled. In our microwave based architecture all laser fields except the detection beams are supplied as sheets and do not have to be precisely aligned or individually controlled.

We present the blueprint for a scalable microwave quantum computer module, which is based on today's silicon semiconductor and ion trap technology. The modules, driven by global laser and microwave fields, perform ion loading, ion shuttling, generate locally addressable magnetic fields as well as magnetic field gradients to perform single and multi-qubit gates and feature on-chip photo detectors for state readout. All gate, shuttling and

state detection operations are controlled by on-chip electronic controls and voltage generation, a cooling system is integrated into the modules and alignment capabilities are integrated with the modules. Each module, when placed in an ultra-high vacuum system and supported by global laser and microwave fields operates like a small stand-alone quantum computer.

Architectures based on photonic interconnects have great potential for scaling up quantum computing [4, 10], however the interaction rate between modules and therefore the speed of a computer based on these is typically slow [13] compared to the execution time of other quantum operations [1, 3, 5]. We propose an alternative method of scaling to a large number of modules based on technology which aligns modules next to each other enabling ion transport between adjacent modules. A universal two-dimensional architecture is formed by fast shuttling [14] of qubits from one module to adjacent modules. A suitable high-error-threshold error correction code that only relies on nearest-neighbour interactions was developed by Fowler et al. [15] and can be implemented using this architecture. We note that the addition of photonic interconnect regions constitutes only a minor adjustments to this blueprint, our module is therefore suitable for the majority of ion trap based quantum computing architectures proposed so far [9, 10].

Our manuscript is structured as follows. A brief overview of microwave based quantum operations is given in Sec. II. The blueprint for individual quantum computer modules is provided in Sec. III. In Sec. IV we discuss how modules can be connected and used to create a universal quantum computer architecture. In Sec. V the surface error correction code, which can be used with this architecture, is discussed and the system size and speed for a 2048 and 1024 bit number Shor factoring algorithm is outlined.

MICROWAVE BASED QUANTUM GATES

Single- and multi-qubit gates, executed with high-fidelity, are essential building blocks of a universal quantum computer. For ion trap quantum computing, internal states of atomic ions serve as qubits, while the Coulomb interaction between closely spaced ions makes conditional quantum gates with two or more qubits possible [16]. In order to couple the dynamics of internal qubit states and motional states, and thus implement multi-qubit gate operations, precisely aligned laser beams have predominantly been used. This has lead to impressive experimental demonstrations of multi-qubit gates with up to 14 ions [17] and the demonstration of a two-qubit gate in the fault-tolerant regime [5]. Nevertheless, there are challenges with the above implementations when trying to scale them up to unlimited numbers of qubits and when trying to increase the gate fidelity further to reduce the overall system size. Technical challenges when operating the large number of laser beams required for a large scale quantum computer systems include the mastering of intensity- and phase fluctuations, frequency drifts of the laser output, micron-precise beam alignment, beam pointing instabilities and non-perfect beam quality. In addition to the technical challenges off-resonant coupling to states outside of the qubit subspace to resonant transitions caused by Raman beams and spontaneous emission can pose an additional problem.

A promising solution to the stability and scalability challenges that come with using lasers to implement large scale multi-qubit gate operations was proposed by Mintert and Wunderlich in 2001 [12], making use of microwave radiation and a static magnetic field gradient. Microwave radiation has since been used to perform single qubit gates with unprecedented fidelity [1, 18], featuring an error per gate in the 10^{-6} range [1] and when combined with locally adjustable magnetic fields or magnetic field gradients, individual addressing of closely spaced ions has been demonstrated with crosstalk as low as 10^{-5} [19].

Coupling between internal states of trapped ions and their motion, necessary for multi-qubit gates, is induced by electromagnetic radiation. Due to the long wavelength (on the order of centimetres) this coupling is vanishingly small for free-running microwaves and is, thus, not useful on its own for multi-qubit gate operations. However, when adding a static magnetic field gradient, which exerts a force due to the magnetic moment associated with the qubit states of the trapped ion, multi-qubit gates can indeed be implemented [12]. Such magnetic field gradient induced coupling was first used to implement a two-qubit gate between nearest and non-nearest neighbours by Khromova et al. [20].

Besides using a static magnetic field gradient to implement multi-qubit gates, one can also make use of microwave near-field gradients [21] which has been demonstrated in the pioneering work of Ospelkaus et al. [22].

A challenge when using the static magnetic field gradient scheme stems from the requirement of the qubit to be made up of at least one magnetic field sensitive state. This limits the achievable coherence time and gate fidelities due to uncontrolled magnetic field fluctuations [20] and measures have to be taken to shield or compensate these fluctuations. An efficient way to obtain qubit states that are robust against field noise is the use of microwave dressed-states [7, 23]. These dressed-states have been shown to exhibit a coherence time three orders of magnitude longer compared to bare magnetic field sensitive qubit states and have already been combined with a static magnetic field gradient to cool a single ion to the quantum ground-state of motion using long-wavelength radiation [24]. Using such quantum engineered clock states, a high-fidelity 2-qubit gate has recently been demonstrated [25] with the method being

capable of producing fault-tolerant quantum gates within the module architecture described in this article.

Static magnetic field gradient induced couplings will be used as a basis for multi-qubit gate operations within individual modules described here.

Recent work has even shown the possibility to cancel the carrier transition permitting much faster gate speeds [7, 26]. For the design of a scalable quantum computer module it is valuable to be able to rely on the matured and commercially developed field of microwave engineering, allowing stable microwave and RF fields to be generated at comparably low cost and, for a typical user, with a fraction of the complexity of laser systems. Long-wavelength radiation can naturally address a large spatial volume, making it very useful when scaling a given operation to many ions.

DESCRIPTION OF INDIVIDUAL QUANTUM COMPUTER MODULES

We propose a blueprint for a scalable quantum computer module, which makes use of the discussed microwave based multi-qubit gate scheme, is fabricated using silicon microfabrication technology and features high speed single qubit and multi-qubit gates using microwave dressed-states. The scalable modules are the basis for a large scale quantum computer architecture and feature microfabricated ion trap X-junction arrays [27–29]. In each X-junction two or more ions are trapped and feature up to three different zones, as shown in Fig. 1: microwave-based entanglement zone, state detection zone and loading zone. Once an ion is trapped in the loading zone, high-fidelity shuttling operations [30, 31] transfer the ion to the entanglement zone. There, ions can be individually addressed using locally adjustable magnetic fields and entangled using static magnetic field gradients in conjunction with global microwave fields. After all single and multi-qubit gate operations required for error correction and logic operations are completed, the ion is transferred to the detection zones, where global laser fields and on-chip photo detectors are used for state detection. All coherent quantum operations are performed and controlled by on-chip electronics relying only on global microwave fields and laser fields. In our microwave based architecture all laser fields except the detection beams are supplied as sheets and do not have to be precisely aligned or individually controlled.

The design of the X-junction, individual zones, control electronic, cooling and alignment system of the modules will be described in detail in the next paragraphs. We start with the core element of the modules, the ion trap X-junction architecture, that allows for fast high-fidelity ion shuttling and separation operations. High-fidelity shuttling through junctions requires a highly optimized electrode geometry [32]. An example for such a junction geometry is shown in Fig. 1, featuring minimal RF barrier and barrier gradient. The optimized electrode geometry is combined with advanced static voltage electrodes designed for fast and efficient shuttling and ion separation, following the work presented in [33]. The RF barrier of the highly optimized X-junction was simulated to be on the order of 0.25 meV for a trap depth of ∼0.1 eV and an ion height of 100 μm. High-fidelity shuttling through X-junctions in a surface trap [31] with similar barrier has been successfully demonstrated. We propose to use very fast ion transport through the junction, similar to the work presented in [14, 30] and fast ion separation demonstrated in [30, 34], combined with sympathetic cooling using a second ion species [35] to achieve a fast quantum computer cycle time.

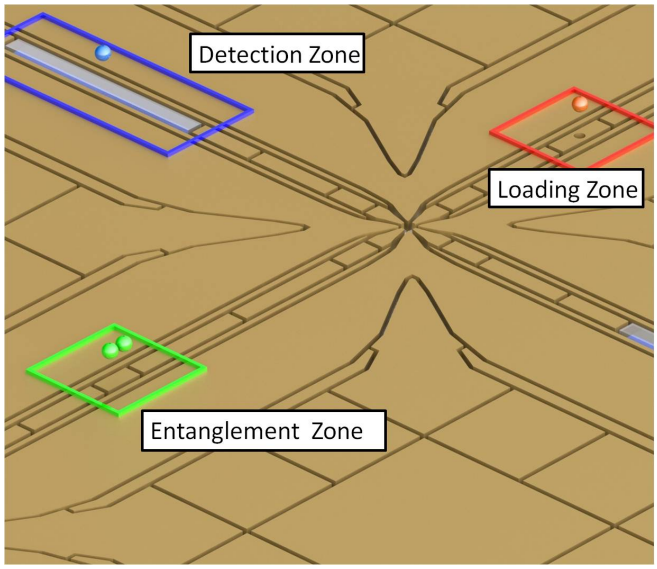

FIG. 1. X-junction featuring multiple zones, including a loading zone (marked red) in selected junctions. Multi-qubit gates are performed bringing two or more ions (green) together in the entanglement zone (marked green). The gates are performed by applying a static magnetic field gradient produced by current wires placed underneath the electrodes. State detection is carried out in the detection zone (marked blue) using global laser fields and photo detectors placed underneath the electrodes.

Static electrodes are connected using proven and developed vertical interconnect access (VIA) and buried wire technologies [29]. Additionally, a structured ground plane layer is used to avoid exposed dielectrics. The microfabricated conductive and insulating layers are placed on a high resistivity (HR) silicon substrate exhibiting minimal RF losses and the layer structure is shown in Fig. 2. Using through-silicon vertical interconnect access (TSV) structures, connections to the static and RF electrodes are made from the back of the structure holding the X-junction. The electronic control system generating the static voltages on the module and allowing for

RF voltages to be supplied via shielded cables will be described in more detail in the electronic control paragraph.

Decoherence caused by transferring the ions through spatially varying magnetic fields are compensated by mapping the magnetic fields in the junctions. Fluctuations of the magnetic field can be detected using ions of a different species sensing magnetic field fluctuations at various positions of the module [36].

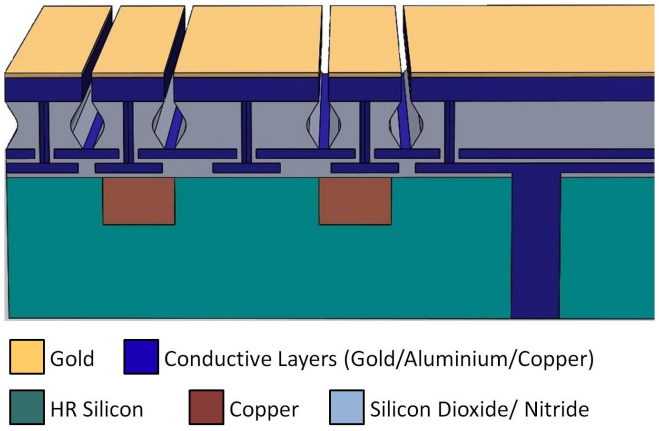

FIG. 2. Layer structure of the monolithic ion trap chips consisting of highly resistive silicon substrate (HR silicon) and copper current wires embedded in the silicon. Conductive and insulating layers form buried wires, vertical interconnects (VIAs), through-silicon vias (TSVs) and electrodes and a gold layer coating the electrodes to prevent oxidization.

Initial loading of ions to the X-junction and to replace lost ions is performed using the loading zones placed in one arm of the X-junctions close to the edge of the modules. Backside loading zones require a global ionization laser beam in combination with an atomic flux originating from the back of the substrate, commonly known as backside loading [37]. The atomic flux is generated by an atomic oven passing through slots fabricated into the silicon substrate and carefully designed centre segmented electrodes, shown in Fig. 1. When an ion is lost from a particular position within a module a new ions is trapped and all ions placed between the position of the lost ion and loading zone are shifted by one position, only requiring a single shuttling sequence.

In another arm of the optimized X-junction an entanglement zone is located that features a strong magnetic field gradient and an adjustable local magnetic field offset. The required magnetic field gradients and fields are generated using current carrying wires embedded in the silicon substrate as shown in Fig. 3. Large static magnetic field gradients of 150 T/m at the ions position [38] are used for fast, high-fidelity microwave gates. To generate these gradients a current of $\sim$10 A is passed through each copper wire. Conductivity and cooling of the silicon substrate and copper wires will be discussed in detail in the cooling system description below. The strong magnetic field gradients work in combination with global microwave fields to perform multi-qubit gates in parallel in the entire quantum computer architecture. Depending on the error correction code used with this architecture, two or more qubits can be entangled in each entanglement zone.

Locally adjustable magnetic fields, generated by additional current carrying wires placed underneath each entanglement section, shown in Fig. 3, are used to individually address every ion in the system in parallel by shifting ions in and out of resonance with multiple global microwave fields of different phases [39]. The on-chip control electronics is based on digital to analogue converters (DACs) and control the current with 16 bit precision and an update rate of >1 MHz. Arbitrarily many different qubit rotations are performed in parallel with ions placed inside the locally adjustable magnetic fields of the entanglement zones. Required microwave frequencies for the global fields are generated by commercial frequency generators, mixers combine all necessary frequencies into one signal and amplifiers supply the signal with sufficient amplitude to emitters inside the system. The entanglement zones perform all quantum operations controlled by in-vacuum electronics and powered by global microwave fields.

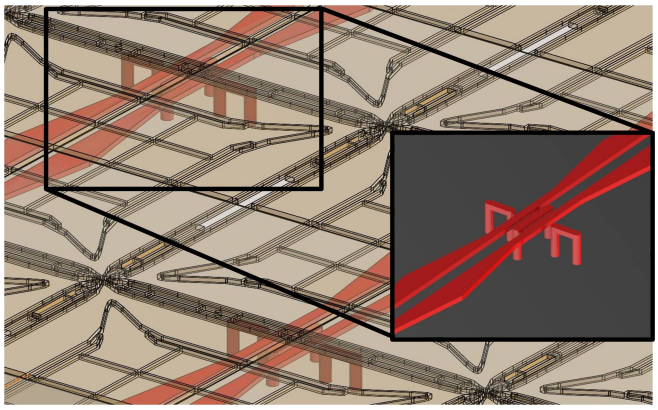

FIG. 3. Illustration showing an isometric view of the two main gradient wires placed underneath each entanglement zone. Short wires are placed locally underneath each entanglement zone to compensate for magnetic field fluctuations and to allow for individual addressing. The addressing wires can be seen in more detail in the inset.

To detect the quantum state of the ions after performing single and multi-qubit gates, detection zones are incorporated into another arm of the X-junction as shown in Fig. 1. In the detection zone, multiple centre segmented electrodes are made of indium tin oxide (ITO) instead of gold. ITO is highly UV transparent and allows the light emitted from an ion placed above the zone to pass through the electrodes. Photodetectors are fabricated onto the silicon substrate and separated from the

electrodes by a highly UV transparent dielectric layer, similar to the concept presented in [40] and shown in Fig. 4. VIA wall structures are used to prevent optical crosstalk from neighbouring detection zones. Commercial silicon based microfabricated photon counters [41] (multi-pixel photon counters, MPCCs) reach quantum efficiencies of ∼30% and are compatible with the proposed silicon substrate. When cooled to 77 K they also show a reduction of dark count rate on the order of 10^5, to ∼1 Hz [42]. The total photon detection efficiency of this detection setup will be on order of 2% assuming an 80% transmission rate of the ITO and dielectric layer and collection efficiency of ∼10%. Detection efficiency and dark count rate are comparable to the values given in [3] and similar state detection fidelity and detection time on the order of 99.9% in 45 μs are expected for this setup.

State detection operations will have to be performed many times during error corrected logical qubit operations. To preserve the state of physical qubits performing these operations only ions placed inside the detection zones are illuminated while ions placed in the entanglement zones are not. Detection and entanglement zones are placed in perpendicular arms of junctions, as shown in Fig. 1. Global laser beams are steered parallel to and between the entanglement zone arms, which are separated by 2.5 mm, only addressing the ions in the detection zones shown in Fig. 4 (b). The required accuracy of the beam steering is readily achieved using in-vacuum optics. Using mirrors for multiple passes of the junction array, one laser beam can cover an entire module.

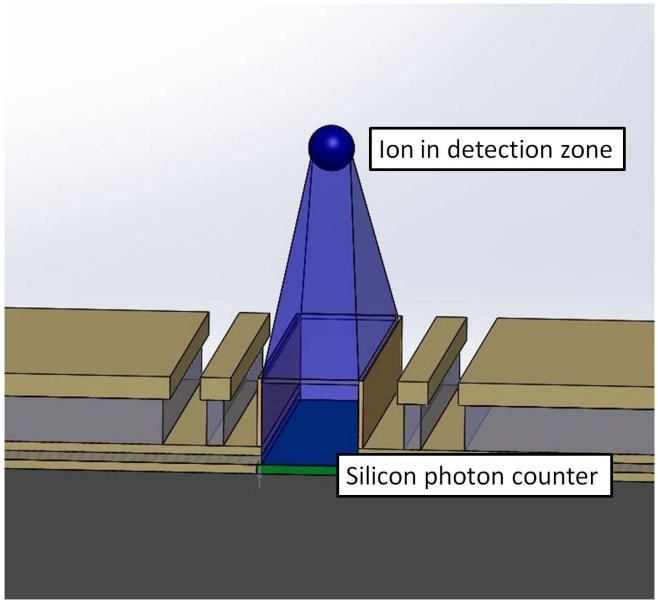

FIG. 4. Silicon photo detector (marked green) embedded in the silicon substrate, transparent centre segmented electrodes and possible detection angle are shown. VIA structures are used to prevent optical crosstalk from neighbouring detection zones.

The X-junction structures equipped with the zones discussed, occupy an area of 2.5×2.5 mm^2 and can be fabricated in large numbers on the same silicon wafer to form the scalable quantum computer modules. If too many X-junctions are electrically connected, the capacitance and power dissipation become too large to be driven with a standard helical resonator of high quality factor [43]. Simulations using the 'Advanced Design System' tool show that by connecting only 6×6 junctions together in one electrical section, the capacitance can be kept below 80 pF and a quality factor of Q> 200 is possible using a compact helical resonator of ∼15 mm. The compact resonators are placed inside the system underneath the modules and connected with shielded precision cables to the electrical sections. All resonators are attached to the same frequency source with ∼25 MHz and the individual resonance frequencies of the resonant circuits are tuned using variable capacitors. Close proximity of the resonators to the electric sections and careful design of the wiring will result in a negligible phase difference between RF electrodes of different electrical sections.

The electrical sections have a footprint of 15×15 mm^2 and feature 1224 static voltage electrodes and 108 individual local gradient current wires. The required static voltages and currents are supplied by DACs inside the vacuum system similar to the concept presented in [44]. In our concept, DACs are fabricated on separate silicon substrates, which are attached to the ion trap substrate using TSV and wafer-stacking [45] technology.

Each wafer layer features 4 DACs with 40 analogue outputs each [46] and combined with the required TSV and RC filters occupy an area of no more than 15×15 mm^2. Generating enough analogue outputs requires a total of 9 wafer layers that will be stacked together. An additional layer is used to house an electronic control unit, which simplifies the digital control of the 36 in-vacuum DACs.

The scalable quantum computer modules are made up of 6×6 such electrical sections, monolithically fabricated onto 90×90 mm^2 HR silicon wafer pieces. The modules feature 1296 individual X-junctions, are controlled by on-chip electronics and perform the require quantum operations using magnetic field gradients, local magnetic fields and global laser and microwave fields. Embedded copper wires generating the magnetic field gradients are routed in such a way that only 4 high current connections are required per module, shown in Fig. 3.

Passing large currents of 10 A through wires with a small cross section ($\sim 30 \times 60$ μm^2) make it essential that the resultant heat is efficiently distributed and transported away from the modules. In addition, the power dissipated by the ion trap structure and the in vacuum electronics needs to also be transported away from the modules. Melting of the wire structures can be avoided by cooling the silicon substrates below 100 K, which results in an extremely high thermal conductivity

($\kappa > 1000\ W/(m{\cdot}K)$) of silicon [47] and an increase of the copper conductivity by a factor of 10 [48]. To estimate the temperature of the copper wires in this design the total heat output per module needs to be calculated first. Considering the heat generated by the copper wires, RF dissipation in the trap structure and power dissipation of the on-chip electronics a maximum heat output per module was estimated to be on the order of 1500 W, which is equal to 0.19 W/mm^2 [49]. The assumed heat output is likely to be significantly lower as the power dissipation of on-chip electronics and ion trap structures are estimated for room temperature. To efficiently remove the heat from the modules a liquid nitrogen microchannel cooler is integrated into the back wafer of the modules. Deep trenches are etched into the backside of the last wafer forming many channels through which liquid nitrogen is passed. The channels are covered using an additional silicon wafer. Fabricating the entire module including the liquid cooler out of silicon prevents additional stress and wafer bow arising from different thermal expansion coefficients.

A similar microchannel cooler has been shown to achieve a heat transfer coefficients of >0.1 W/($mm^2{\cdot}$K) [50], which is sufficient for this system. Based on the total heat dissipation, thermal conductivity of silicon wafers and copper interconnects, the thermal gradient between the copper wires and the coolant through the multi wafer package and microchannel cooler will be only ∼3 K, preventing the copper wires from melting. Liquid nitrogen, which is cooled from 77K to 65K to prevent boiling inside the microchannel cooler, will be used as coolant and is supplied to the modules using multiple UHV compatible flexible steel tubes. Continuous flow liquid nitrogen coolers are commonly used for detectors and if designed correctly introduce minimal vibrations to the system [51].

Each of these modules can work as a stand-alone small scale quantum processer modules, featuring 1296 X-junctions, entanglement and detection zones. If one wants to perform a computationally hard problems, such as Shor factorizing a 2048bit number a much larger architecture, consisting of many modules will be required. Each module will have to be interfaced with each other to create a universal quantum computer architecture. The approach presented by Monroe et al. [9] makes use of photonic interconnects and commercial fibres to interface arbitrarily many modules. This approach has great potential, but the speed of such a system is currently limited by the interaction rate between modules [13], which is typically much slower than other quantum operations [1, 3, 5] performed by the modules.

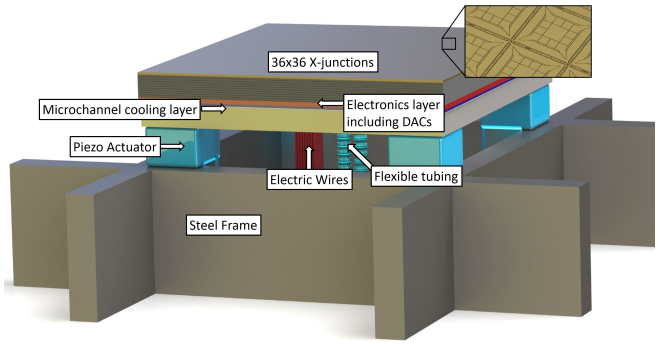

FIG. 5. One module consisting of 36x36 junctions placed on the supporting steel frame structures: Nine wafers containing the required DACs and control electronics are placed between the wafer holding 36x36 junctions and the microchannel cooler (red layer) providing the cooling. X-Y-Z piezo actuators are placed in the four corners on top of the steel frame. Flexible electric wires supply voltages, currents and control signals to the DACs and control electronics. Coolant is supplied to the microchannel cooler layer via two flexible steel tubes placed in the centre of the modules.

SCALING MODULES TO A UNIVERSAL QUANTUM COMPUTER ARCHITECTURE

We are proposing an alternative scheme that does not rely on photonic interconnects and is therefore not limited by the interaction rate of these. In our scheme, modules must be assembled in such a way that ions can be directly transported from one module to another. RF and static voltage electrodes thus need to be fabricated all the way to edge of the modules so that the electric fields confining the ions reach beyond the edges. The modules must also be accurately aligned so that two neighbouring modules create an overlapping continues electric field, suitable to trap ions at any position. If such an electric field can be created, ions can be transported from one module to another and the resulting two dimensional module array will feature faster interaction rates and system clock cycles, without requiring special interaction zones. The challenging part of our scheme is to accurately align all the modules to each other and to prevent large barriers or interruptions of the overlapping electric fields to occur.

Experimentally, it will not be possible to align all modules perfectly to each other and there will be a misalignment between the RF electrodes of neighbouring modules. We have therefore performed multiple boundary element method (BEM) electric field simulations of the misaligned three dimensional trap structures to investigate the feasibility of shuttling ions from one module to another taking account of expected misalignment be-

tween adjacent modules. We analysed the electric potential and RF barrier caused by RF rails misaligned in different directions and magnitude. Results of the simulations show that an RF barrier occurs, similar to the one found in an X-junction centre. Misalignment in one or two dimensions causes a lower barrier than misalignment in all three dimensions and the barrier height is dominated by misalignment in the direction perpendicular to the trap surface. Assuming a worst case of a misalignment in all three axes by $\leq$10 μm, the simulated RF barrier was found to be $\sim$0.2 meV, as shown in Fig. 6, for a trap depth of $\sim$0.1 eV and an ion height of 100 μm. The barrier of 0.2 meV is of similar height to the one found in our optimized X-junction centre and the one presented in Ref. [31], where high-fidelity shuttling was successfully demonstrated. Shuttling fidelities comparable or higher than through the X-junction centres are expected if the RF voltages applied to both modules show no significant phase or frequency difference.

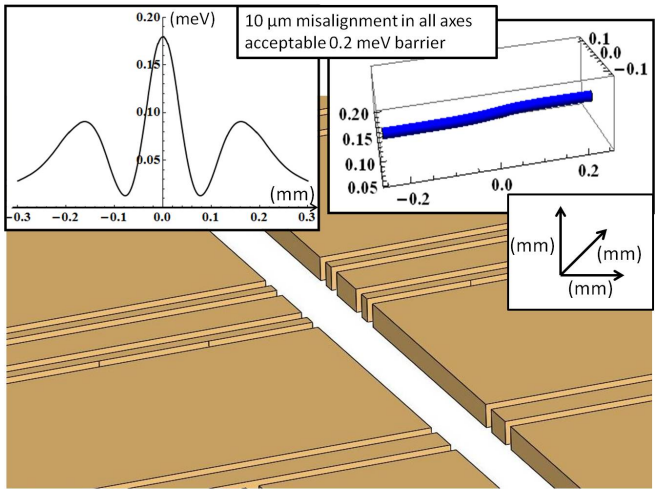

FIG. 6. Two modules misaligned in the x-y-z axes by 10 μm each and the corresponding RF pseudopotential minimum (marked blue) and RF barrier in meV along the RF nill.

As discussed in the previous section, all resonators providing the RF voltages to the modules are connected to the same frequency source. Also all modules will feature the same path length and impedance of the coaxial connections from the resonators to the RF electrodes. This will lead to a negligible RF phase difference of the electric fields generated by adjacent modules, which could otherwise weaken the trap depth at the intersection between modules. Micromotion induced by the RF phase mismatch is not expected as the phase difference would occur between adjacent and not parallel RF electrodes.

To achieve an alignment of the modules of $\pm 5\mu$m in three dimensions, limiting the RF barrier to the discussed $\sim$0.2 meV, multiple UHV and cryogenic compatible X-Y-Z piezo actuators are attached to the bottom of each module. The illustration in Fig. 5 shows a pictorial representation of a single module of the scalable architecture including required connections and attached piezos. The exact positions of the modules are determined using microfabricated diffraction gratings on the front of the modules and a laser measurement system. After the alignment system determines the position of each module, the modules are accurately positioned in all 6 axes to each other using the piezo actuators. Our architecture is three orders of magnitude less demanding in alignment precision than lithography stepper systems, where 3-5 nm alignment precision in vacuum is routinely achieved (ASML TWINSCAN NXE:3300B).

The discussed alignment capability would be severely hindered if the modules are strongly warped in random directions or the edges of the modules are not precisely fabricated. Due to the high thickness of the silicon wafer modules (on the order of 10 mm) negligible wafer bow is expected and the bow will also be characterized for every modules before assembly. The edges of the modules are created using high resolution photolithography and anisotropic dry etching (Bosch process). These process steps, which are commonly used in the microfabrication of microchips and MEMS devices, reach sub μm precision and will not limit the alignment capabilities.

Each steel frame can hold on the order of 1708 modules and is accurately placed inside large octagonal shaped UHV chambers ($\sim$ 4.5 $\times$ 4.5 m^2 large). The chambers hold one steel frame each and feature viewports on the sides and top for allowing optical access, see Fig. 7. Imaging, beam shaping and guiding the laser light fields above the trap surfaces is achieved using in-vacuum optics. Each chamber also incorporates all required feedthroughs for currents, static voltages, RF and microwave signals, coolant and digital control signals. In addition, the chambers are equipped with liquid nitrogen cooled copper shields and a variety of vacuum pumps to create an ultra high vacuum environment. Multiple chambers can be directly bolted together creating one large universal quantum computer of arbitrary size. Each chamber of such a vacuum system, shown in Fig. 7, can hold $\geq$ 2.2 million individual junctions.

SURFACE ERROR CORRECTION CODE

Performing computationally hard problems in a quantum computer, such as prime factoring of a 2048 bit number, involves so many qubits and logical operations that even the smallest error probability per operation will prohibit a successful outcome. Quantum error correction, which uses multiple physical qubits to create logical qubits with a much lower error rate, is thus a necessity for scalable quantum computing. Following the pioneering work by Steane [52] and Shor [53], a variety of different error correction strategies have been developed.

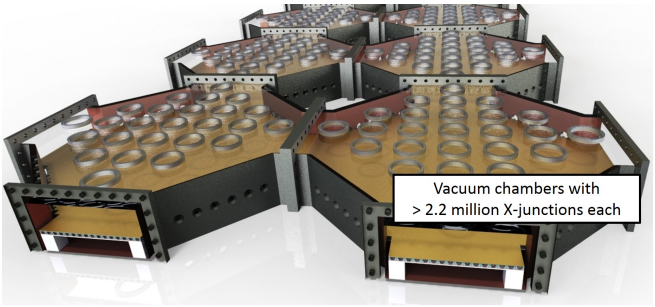

FIG. 7. Schematic of octagonal UHV chambers connected together, each chamber is 4.5x4.5 m^2 large and can hold > 2.2 million individual X-junctions placed on steel frames.

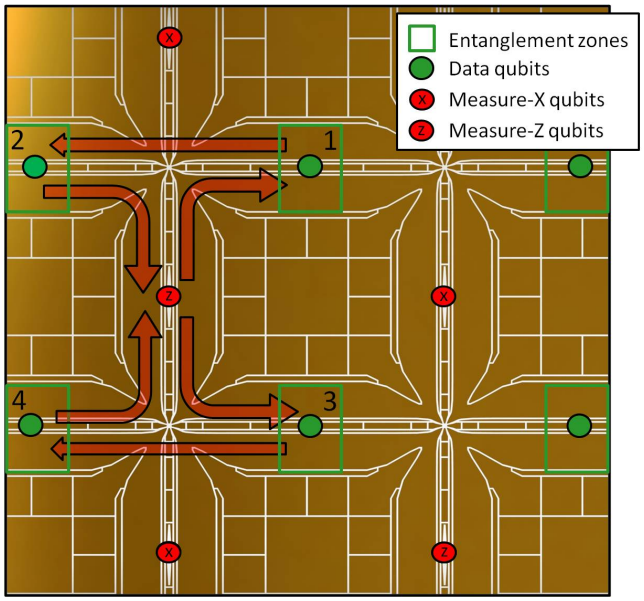

FIG. 8. Small section of the scalable architecture illustrating how data and measurement qubits interact with each other in the entanglement zones to execute the surface code. Data qubits are static and measurement qubits are shuttled to all adjacent entanglement zones.

In the original proposals, logical qubits were encoded in a smaller number of physical qubits using special code word states that allow identification and fixing of errors (occurring on single physical qubits) without destroying the logical qubit states. These codes require the error probabilities associated with each operation on the physical qubits to be limited to a very challenging level (of order 10^{-5}) for the error code to work.

Since then, schemes have been developed that can tolerate much larger error probabilities, but rely on the coding of logical qubits in a larger number of physical qubits. One such scheme is the surface error correction code described by Fowler et al. [54], which tolerates error probabilities of each operation up to 10^{-2} and relies only on nearest neighbour interactions. We will briefly summarize how the surface code protects from errors, discuss how it can be implemented with our two-dimensional array architecture and how it can be used to perform fault-tolerant logic operations.

The surface code requires physical qubits to be placed in a regular lattice, that we can decompose into one sublattice holding so called data qubits and another sublattice holding measure-X and measure-Z qubits. In our architecture, two ions are trapped in each X-junction section, as shown in Fig. 8. One ion is permanently placed in the entanglement zone constituting the data qubit, the second ion is alternatively a measure-X or measure-Z qubit, placed in the detection zone and can be shuttled to the four adjacent data qubits.

Measure-X and measure-Z qubits constantly monitor the states of their four nearest neighbour data qubits. The measure-Z qubits perform four successive CNOT gates with the data qubits in their respective entanglement zones, in the order displayed in Fig. 8, after which the state of the measure-Z qubit is detected. The measure-X qubits perform almost the same sequence, but an additional Hadamard gate is applied to them before and after the four CNOT gates. The measure qubit sequence is run simultaneously in a synchronized manner with all measure qubits of the entire architecture and repeats itself over and over again throughout the calculation.

Associated with each four CNOT gate sequence are the products of four σ_x or σ_z Pauli operators for the measure-X or measure-Z qubits respectively. The eigenstates of the products are dependent on the four neighbouring data qubits and all products commute with one another. For a single arbitrarily sized two-dimensional array of qubits, only two states exist which are joint eigenstates with eigenvalue +1 of all these operators. These two eigenstates are the surface code states of the two-dimensional array and constitute the logical qubit states $|0\rangle_L$ and $|1\rangle_L$.

If a single data qubit of the array undergoes an error, either the projection performed by the measure qubits corrects it or the error is detected by measuring the states of the four neighbouring measure qubits. The error could then be corrected, but an easier and more robust way is to merely store the error information. The correction can then be performed 'in software', i.e., by translating the measurement results at the end of execution into the appropriately modified values.

Should ions be lost from the qubit space due to entering a dark state, optical pumping is used to drive them back to the qubit space and the net effect is then equivalent to a qubit error of the form detected and corrected by the code. Complete loss of a measure qubit due to collisions with background gas is detected due to the periodic state detection of these after each measurement

cycle. When such a loss is detected, the empty measure qubit site is replenished with a new ion from one of the loading zones by shifting all ions between the loading zones and the empty measure site. The loss of a data qubit cannot be detected directly and we propose to use the measure qubit as indicator if a data qubit is present in the entanglement zone or not.

When the measure qubit is shuttled into the entanglement zone, it will experience different electric potentials if a data qubit is present. If the data qubit is present, the two ions occupy left and right potential minima, while if the data qubit ion is missing, the measure qubit will occupy the centre of the potential well. When shuttling the measure qubit out of the entanglement zone a special potential well is applied that leaves measure qubits placed in the centre of the well in the zone, while off-center measure qubits are extracted and the measurement cycle proceeds. The measure qubit replaces missing data qubits automatically and is replenished in a later cycle using the previously discussed method. Typically after a single execution of the measurement cycle, the surface code is re-established.

A two-dimensional array where all data qubits are error corrected at all times can accommodate only one logical qubit. To implement multiple logical qubits in such an array, one can simply turn off the detection carried out by two measure-X or -Z qubits at a distance of a few sites. Turning off measure qubits removes constraints and adds more states to the state space of the array. These states, which are still distributed over all the ions, define the logical qubits created [54].

Logical one- and two-qubit gates are implemented by so-called braiding operations, which are described in more detail in Ref. [54]. Braiding operations can be implemented in our surface code protected architecture by turning on and off multiple measure qubits in such a way that they form paths (braids) that lead from the measure qubits, defining one logical qubit, around the measure qubits defining another logical qubit, and back. After a complete cycle where the measure qubits are turned on again along the same path, a logical two-qubit gate is effectively implemented on the logical qubits. While performing such a logical qubit gate the data qubits remain in their entanglement zone and the turned off measure qubits are 'parked' in their detection zone. In the rest of the array, the previously described measure qubit sequences are continuously performed, no additional operations have to be performed.

Non-Clifford single qubit $\pi/8$ Z-rotations are the most challenging operations to implement with the surface code. In Ref. [54], it is proposed to implement these single-qubits gates by performing logical two-qubit CNOT gates using ancilla qubits which are logical qubits initialized in states of the form $|0\rangle_L + e^{i\pi/4}|1\rangle_L$. Logical qubits can not be directly initialized to such a state performing only logical gate operations. It was therefore proposed [54] to perform the required rotations on the physical state of one data qubit. The data qubit state is then 'injected' into an error corrected logical qubit. Simplistically, a logical qubit consisting of only one data qubit is created and the rotation is performed on the data qubit state defining the logical qubit state. Afterwards the logical qubit is 'grown' to achieve the desired fault tolerance again. Although the initialized state is now error protected, the original operation creating the state was performed on a physical qubit and does not have a low enough error probability for performing computationally hard problems. Therefore it is necessary to create multiple logical qubits with the same injected states and to use an error correction code like the Steane code to distill them to high-fidelity. The Steane code is implemented using the surface code logical qubit operations and produces logical ancilla qubits, which are needed in large numbers. Their production with adequate precision is estimated to occupy more than 90% of all physical qubits of the system [54].

By implementing and amending the surface code scheme to accommodate one measure and one data qubit ion in all X-junctions of our architecture, we have the necessary ingredients to employ the scheme analyzed in detail in [54]. We assume the same gate and memory error probability of 0.1%, which we expect to be achieved when implementing the microwave gate scheme with the proposed magnetic field gradient. Based on the same scheme we can give quantitative estimates on the system size and processing time for a machine that solves a relevant, hard problem, such as the Shor factoring of a 2048 bit number. For the calculations we assume a single qubit gate times of 2.5 μs, a measurement time of 25 μs and total error correction cycle time, which includes shuttling and two qubit gates times, of around 125μs. Based on these numbers, performing a 2048 bit number Shor factorisation will take on the order of 110 days and require a system size of 10^9 trapped ions. Shor factoring of a 1024 bit number will take on the order of 14 days. Both of these factorizations will require almost the same amount of physical qubits as the required pace of the ancilla qubit generation is the same for a 2048 bit and a 1024 bit factorization. Trapping 10^9 ions will require 15×15 vacuum chambers occupying an area of ca 67.5×67.5 m^2.

We believe that these numbers are very encouraging, and we are confident that further improvements could bring down the overhead of performing such a calculation by up to a factor of ten. Assuming that it will also be possible to reduce the error rate of each quantum operation below 0.01%, it would be possible to perform the 2048 bit number factorization in approximately 10 days, requiring on the order of $3 * 10^8$ ions. In addition one could implement medium-range shuttling, of approximately 30 junctions, which could lead to a further reduction of the required qubits to $3 * 10^6$ ions or $1.5 * 10^6$ X-junctions. These improvement could be implemented without ma-

jor changes to the modules or the architecture and all required qubits would fit into four vacuum chambers.

CONCLUSION

In conclusion, we have described an industrial blueprint for a microwave based ion trap quantum computer, based on modules that are connected via ion transport forming a fully scalable architecture.

We have elaborated how magnetic field gradients in conjunction with global microwave fields can be used to perform multi-qubit gates. Local adjustable magnetic fields in combination with a global microwave field can be used for selective addressing of arbitrary many zones in parallel. We discussed how microwave based single and multi-qubit gates have the advantage of negligible spontaneous emission, possible suppression of the carrier transition and when scaling to a large system allow to replace thousands or millions of laser beams with a few microwave emitters, making this technology ideal for large scale quantum computer architectures.

We then presented the blueprint for a scalable module based on microwave quantum logic, which combines the advantages of microwave based quantum gates with on-chip control electronics, which not only generate voltages to perform shuttling operations but also control quantum operations. When placed in a vacuum system, which supplies the modules with static and RF voltages, coolant and global laser and microwave fields, each module can work like a small stand-alone quantum computer. Design, construction and operation of the modules are discussed in detail and we also described how these modules can be used to form a universal quantum computer architecture. To form such an architecture we proposed an alignment technique, where piezoelectric actuators are added to the modules making it possible to align a module with an adjacent one. The resulting system features nearest neighbour interactions spanning across the entire architecture, making it suitable for an error correction code like the surface error code. By adding photonic interconnect regions, which poses a minor adjustment to the blueprint, the modules can also be used in scalable quantum computing architectures based on photonic interconnects.

Furthermore, we discussed the basic working principle of the surface error correction code and how it can be implemented with this architecture, followed by an estimate for the system size and execution time for performing a 2048 and 1024 bit number Shor factorization.

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