Characterization and reduction of microfabrication-induced decoherence in superconducting quantum circuits

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Many superconducting qubits are highly sensitive to dielectric loss, making the fabrication of coherent quantum circuits challenging. To elucidate this issue, we characterize the interfaces and surfaces of superconducting coplanar waveguide resonators and study the associated microwave loss. We show that contamination induced by traditional qubit lift-off processing is particularly detrimental to quality factors without proper substrate cleaning, while roughness plays at most a small role. Aggressive surface treatment is shown to damage the crystalline substrate and degrade resonator quality. We also introduce methods to characterize and remove ultra-thin resist residue, providing a way to quantify and minimize remnant sources of loss on device surfaces. © 2014 AIP Publishing LLC. [http://dx.doi.org/10.1063/1.4893297]

Improving the coherence times of superconducting qubits is of central importance for pushing quantum integrated circuits to a practical level of fault-tolerance for quantum computation,[1–4] as even moderate improvements to coherence can drastically reduce the overhead required for quantum error correction.[1,4] Substantial evidence has pointed to dielectric loss and fluctuations due to two-level system (TLS) tunneling defects[5,6] as a source of energy relaxation in superconducting qubits and noise in sensitive superconducting photon detectors.[7–18] These studies strongly suggest that TLS defects are located not in the bulk, but at the interfaces between device substrate, metal and vacuum, and that they can vary significantly with device materials, though the precise reason for this variation is usually a matter of speculation. The impact of TLS can be mitigated by increasing circuit dimensions,[9,14,19,20] but this strategy cannot be continued indefinitely. Nonetheless, the variable nature of the TLS-hosting interfaces has not been carefully analyzed.

Here, we use superconducting resonators as sensitive probes to study TLS dielectric loss as a function of the methods used to construct these circuits, while concurrently analyzing the substrate-metal (S-M), substrate-vacuum (S-V), and metal-vacuum (M-V) interfaces. We separately extract the TLS contributions of chemical contamination and induced disorder at the S-M interfaces of superconducting aluminum coplanar waveguide (CPW) resonators, and show how traditional processing methods can limit internal quality factors Q_i to the range of 10^5–10^6 at single-photon powers where TLS effects dominate. In addition, by characterizing resist residue we predict that without careful post-processing techniques, residual polymer films on the vacuum interfaces may soon start to limit superconducting qubit lifetimes.

We expect that measurements of resonator Q_i will predict dielectric loss in similarly fabricated superconducting qubits for two reasons: superconducting CPW resonator Q_i are limited by energy relaxation and indicate excitation lifetimes T_1 at single-photon powers,[10,18,21] and the large single-layer shunt capacitors of many superconducting qubits, such as the transmon, have interface participation ratios and hence dielectric losses comparable to those of a CPW.[16,19,22,23]

Transmon qubit capacitors are traditionally fabricated using lift-off Al deposited together with their double-angle-evaporated Josephson junctions: first a ground plane is etched at the desired location of the qubit, and then electron-beam lithography (EBL) is used to define the qubit pattern that is subsequently evaporated onto the etched substrate.[24–26] This means that the capacitor's S-M interface sees more processing than it would if the capacitor were formed by a subtractive etch alone. Improved coherence times have recently been found in transmons using lift-off metal for only a small fraction of the qubit,[16,17] where the capacitors are first formed by an etch and the Josephson junctions later evaporated after ion-milling the initial layer to remove native oxide and establish superconducting contact. In this process, only a small fraction ($\sim$1%) of the qubit self-capacitance is formed with lift-off metal,[27] and any extra dielectric loss induced by lift-off processing should be reduced by a similar factor. A systematic test to compare these two processes while keeping other parameters constant, including metal type and growth conditions, could reveal information useful for further improvements to coherence.

We perform such a controlled study by comparing Q_i of CPW resonators fabricated with transmon-style lift-off versus a pure etch, both on the same chip, as follows (full details of the fabrication process can be found in the supplement[28]). Photolithography and a dry etch are used to define $\lambda/2$ CPW resonators coupled to a feedline in an Al film deposited on sapphire [Fig. 1(a)]. During the etch, the CPW structure is defined for purely etched control resonators, whereas the full ground plane slot of width $W + 2G$ is etched away for "lift-off resonators;" the center traces of these resonators are defined later using PMMA-based EBL and lift-off [Fig. 1(b)], mimicking traditional transmon fabrication.[28]

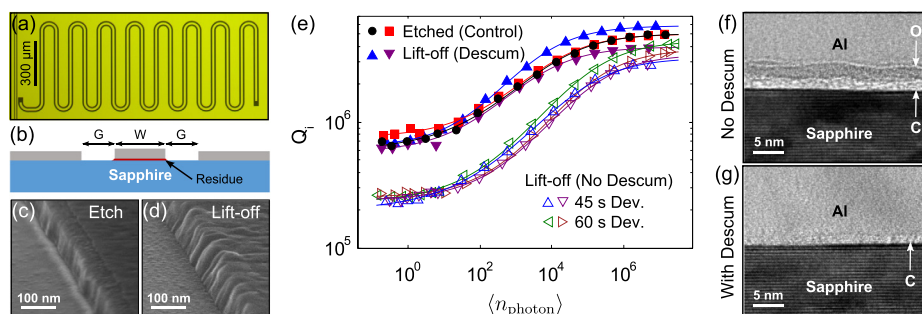[a]Electronic mail: martinis@physics.ucsb.edu

FIG. 1. Etch versus lift-off, and descum versus no descum: low-power Q_i is degraded using lift-off without descum. (a) Optical micrograph of a "hanging" $\lambda/2$ CPW resonator capacitively coupled to a feedline (left). (b) Schematic of lift-off resonator cross section. (c)/(d) SEM image of center trace edge of etched/lift-off resonator. (e) Plot of Q_i versus mean photon population for resonators made with lift-off with and without a pre-deposition descum, as well as for etched control resonators. Different marker types are distinct resonators. Solid lines are guides to the eye. (f)/(g) Edge-on cross-sectional HRTEM image of S-M interface that saw processing similar to that of the lift-off resonators without/with descum. Elemental peaks[28] in C and O from qualitative EELS scans across the interfaces are indicated.

After e-beam resist development, the wafer is optionally treated with a downstream oxygen ash descum before center trace deposition, during which the heated substrate sees purely chemical cleaning, but not ions or plasma.[28] The wafer is then transferred to the same evaporator that provided the initial ground plane, and the lift-off resonator center traces deposited and excess metal lifted off.[28]

The resonator chip is wirebonded into an Al sample box, which is mounted on the 50 mK stage of an adiabatic demagnetization refrigerator equipped with sufficient filtering and shielding so that radiation and magnetic vortex losses are negligible.[15,29] All resonators had $W, G = 15, 10\ \mu$m with frequencies near 6 GHz. Using a feedline[15] allows us to reproducibly extract Q_i for multiple lift-off and etched resonators on the same chip. The resulting Q_i are shown in Fig. 1(e). The decrease and saturation of Q_i at low powers for all resonators is consistent with TLS-dominated loss. A clear difference (factor of 3) is observed in low-power Q_i between the etched resonators and the lift-off resonators without descum, the latter yielding lower Q_i. The descum increases the lift-off low-power Q_i nearly back to that of the control resonators. This suggests that the differing resonator edge profiles [Fig. 1(c)/1(d)] had a negligible effect on loss at this level.[28] It is also apparent that S-M roughness had a minimal effect on loss: the substrate under the center trace of the lift-off resonators was previously etched and is three times rougher than that under the center trace of the control resonators.[28]

To help understand the increased loss in the lift-off resonators, which we attribute to a contaminated S-M interface, we use cross-sectional high-resolution transmission electron microscopy (HRTEM) to examine the S-M interfaces of samples that saw similar[28] processing to the center traces of the lift-off resonators without/with the descum [Fig. 1(f)/1(g)]. With no descum, we observe two sublayers at the S-M interface. Directly above the substrate is a film of average thickness 1.6 nm, presumably residual resist polymer, which shows a peak in C content when probed with electron energy loss spectroscopy (EELS). Above this, a $\sim$2 nm layer with similar phase contrast to AlO$_x$ is observed, accompanied by a peak in O content when probed with EELS. This layer is likely formed by a reaction of unpassivated Al with resist and/or solvent residue either as the metal is evaporated onto the substrate, or during a later processing step when the wafer

is heated. As such, it may contain impurities such as H that may increase dielectric loss through the introduction of TLS.[7,30–32] Oxide contamination from residue may also be relevant to experiments finding that submicron Josephson junctions are made significantly stabler by cleaning the substrate with oxygen plasma before metal deposition.[33,34]

The S-M interface of the descummed substrate shows a decreased average thickness[28] of carbon-containing residue and no observed peak in O content. Our data are not sufficient to determine if the decrease in carbon residue is in direct proportion to the increase in Q_i.

In situ descum techniques such as ion beam cleaning may perform similarly to the *ex situ* downstream ash explored here. However, as this involves physical bombardment, a cleaning which is too aggressive might degrade the substrate quality at the interface. To test this hypothesis independently from questions of lift-off resist residue, we fabricate etched $\lambda/4$ CPW resonators whose substrates saw different strengths of *in situ* Ar ion beam cleaning prior to the base Al deposition: a weak clean and a stronger mill.[28] The parameters of the strong mill are identical to those used to etch away native AlO$_x$ in the fabrication of Xmon qubits[16] and similar to those used for substrate preparation in other superconducting resonator experiments.[35] The resulting resonator Q_i are shown in Fig. 2(a), and show a power dependence consistent with TLS-dominated loss at low powers. We observe a clear difference (factor of 2) between the low-power Q_i, with the *stronger* ion beam yielding a lower Q_i.

Fig. 2(b)/2(c) shows cross-sectional HRTEM images of the S-M interface for the weak/strong ion beam treatments. The strong mill creates a $\sim$1.2 nm interfacial layer, significantly thicker than the weakly treated interface of unresolvable thickness. EELS reveals no measurable elemental peaks at either interface, including Ar, C, and O. We do not believe the uniform interface is an artifact of surface roughness, as AFM scans reveal no change in roughness between a bare and a strongly milled wafer. We therefore attribute the excess loss to TLS induced by sapphire amorphization. Using finite-element COMSOL simulations,[19] assuming a relative permittivity $\epsilon_r = 10$ for this layer we extract an intrinsic TLS loss tangent $\delta_{\mathrm{TLS}}^0 \sim 1 \times 10^{-2}$.[28]

Returning to Fig. 1(f), one may ask which of the interfacial sublayers of the lift-off resonators without descum
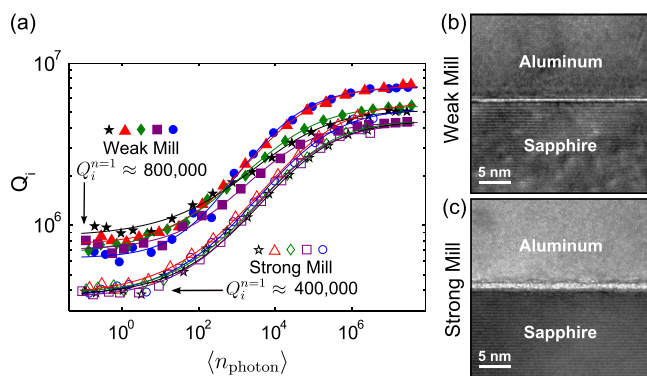
FIG. 2. Comparison of weak and strong ion beam treatment, the latter inducing resonator degradation. (a) Q_i of etched CPW resonators whose bare substrates saw weak or strong *in situ* ion milling before base metal deposition (five resonators of each). (b)/(c) Cross-sectional HRTEM of S-M interface for weak/strong ion mill, showing thicker disordered interfacial layer for strong mill.

dominates the added loss. COMSOL simulations suggest that this added loss could be explained by a 2 nm thick interface with $\epsilon_r = 2$ (e.g., e-beam resist) and $\delta_{TLS}^0 = 3 \times 10^{-3}$, or with $\epsilon_r = 10$ (e.g., AlO$_x$) and $\delta_{TLS}^0 = 1.5 \times 10^{-2}$. In light of this, we more directly extract δ_{TLS}^0 for the contamination by trapping it in a parallel plate capacitor, as illustrated in Fig. 3. The bottom plate of the capacitor (formed by part of the Al ground plane) is thoroughly cleaned, and then PMMA copolymer e-beam resist is spun, exposed and developed, after which the top capacitor plate is deposited along with the CPW center trace, trapping any residue. By forming a large (but physically small and thus lumped element) load capacitance C_L at the end of a $\lambda/4$ CPW transmission line resonator, its net capacitance and loss tangent can be extracted from the shift in resonator frequency and the quality factor. We derive expressions for the load-dominated frequency shift and quality factor in the limit $C_L \gg C_{CPW}$, where C_{CPW} is the total capacitance to ground of the CPW segment of the resonator. We model the lossy load capacitor as an ideal capacitor with an effective series resistance, $R_{ESR} = \tan \delta / \omega C_L$. For a single-dielectric C_L,

$$\omega_r - \omega_{\lambda/4} \approx \frac{2}{\pi C_L Z_r}, \quad Q \approx \frac{1}{2 \tan \delta} C_{CPW} C_L \omega^2 Z_r^2. \quad (1)$$

Numerical SPICE simulations indicate that these expressions are accurate to 1% and 5%, respectively, for our experimental
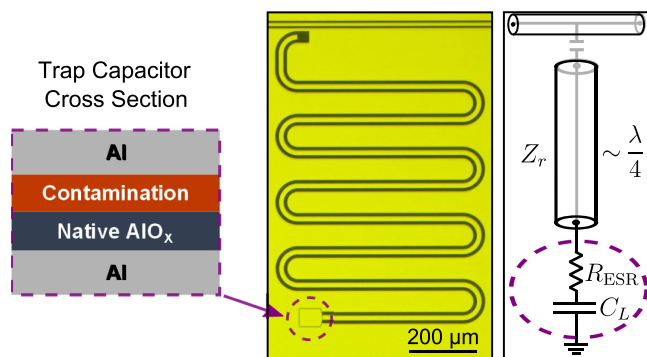

FIG. 3. Schematic of "trap capacitor" experiment to characterize resist contamination. Left: capacitor cross-section. Middle: Optical micrograph of device. Right: Equivalent circuit diagram.

conditions. For a capacitor with more than one dielectric layer, voltage division allows one to extract the capacitance and tan δ of one layer given those of the other. Using this fact and accounting for uncertainty in thickness (3.3–4.0 nm),[28] ϵ_r (9–10), and δ_{TLS}^0 (0.7–1.6×10^{-3})[7,30,36,37] of the bottom native[28] AlO$_x$ layer, we conclude that the net low-power δ_{TLS}^0 of the contamination is in the range of 1.6–3.6×10^{-3}.

We can compare this loss tangent with that of bulk e-beam resist at low temperature and power. To measure δ_{TLS}^0 of bulk resist, we spin-coat CPW resonators with 500 nm of copolymer and use the same bake as for EBL.[28] From the resulting frequency shifts and low-power Q_i of $\lambda/4$ CPW resonators with multiple geometries, we extract (by simulating the capacitance per unit length of the coated resonator cross sections in COMSOL) for the copolymer $\epsilon_r = 2.6 \pm 0.1$ and $\delta_{TLS}^0 = (5.1 \pm 0.3) \times 10^{-4}$. This loss is too small to quantitatively predict δ_{TLS}^0 of the contamination layer extracted from the lift-off resonators or the trap capacitor. We conclude either that the lift-off loss comes from the oxide sublayer [Fig. 1(f)] or that δ_{TLS}^0 of residue exposed to an e-beam is higher than that of the bulk polymer.

To test the effect of exposure, we expose the resist-coated chip in deep ultraviolet (DUV) light sufficient to expose copolymer for development.[28] We then repeat the measurements, observing a modestly increased bulk δ_{TLS}^0 of $(7.7 \pm 0.5) \times 10^{-4}$ with no measurable shift in ϵ_r, still insufficient to quantitatively explain the contamination loss. Although PMMA has a very similar polymer fragmentation pathway and molecular weight distribution upon DUV exposure as it does for e-beam exposure,[38] ultra-thin polymer films may have significantly different TLS properties from the bulk, due, for example, to interaction with the substrate.[39–41] We are thus unable to definitively conclude whether the polymer itself or contaminated AlO$_x$ dominated the lift-off loss.

The question of oxide contamination deserves further study, but in any case, it would be useful to detect and remove residual polymer, including on the vacuum interfaces. Previous interface participation simulations[19] have focused on interfacial $\epsilon_r = 10$, for which the S-M and S-V interfaces participate equally and the M-V interface (i.e., surface oxide) is negligible. However, as shown in Fig. 4, the relative dielectric participation of the three CPW interface types depends strongly on the effective interfacial ϵ_r. Note that S-M contamination is particularly detrimental at low ϵ_r. We also see that post-processing residue on the substrate and even on the metal may start to limit coherence near the 100 μs level for planar transmon qubits of modestly large size. It would therefore be useful to characterize the presence of residual films.

To detect and eliminate post-processing residue, we use variable angle spectroscopic ellipsometry to measure, on various surfaces, the ultra-thin residual films left by unprocessed e-beam resist and photoresist. Here, the resist is spin-coated onto a clean surface, baked, and then stripped. The results are summarized in Table I and are reproducible. We observe that the e-beam resist leaves substantially more residue than the photoresist, perhaps in part due to its higher bake temperature (160 °C versus 95 °C), justifying the assumption of 3 nm for the S-V and M-V interfaces in Fig. 4, although the
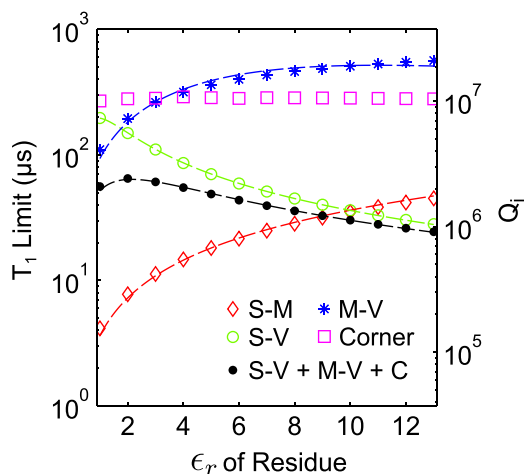
FIG. 4. Markers: COMSOL simulations of $T_1 = Q/\omega$ limit at 6 GHz due to loss at the different types of CPW interfaces (considering separately "corners" where the interface types intersect[19]) as a function of ϵ_r of the interface, assuming a $W, G = 15, 10\,\mu m$ untrenched CPW resonator with 3 nm thick interfaces of $\tan\delta = 2 \times 10^{-3}$, with $\epsilon_r^{substrate} = 10$. Lines are fits to a simple model.[19]

nature of leftover resist residue may depend strongly on any previous processing steps. Ultra-thin residue at the vacuum interfaces, then, may soon start to affect transmon lifetimes.

From Table I, it is evident that some form of oxygen treatment is needed to completely remove the residual films. Note that UV-ozone cleaning (row 4) is an effective method that does not involve heating the substrate, which may be preferable for post-processing devices with Josephson junctions.[34] We do not observe any statistically significant change in Q_i at the $\sim 1 \times 10^6$ level after post-downstream-ashing the etched control resonators (which saw e-beam resist). Higher-quality epitaxial Al resonators[15,42] would be necessary to detect improvement or degradation due to this vacuum-interface residue or post-downstream-ashing. We do however observe a significant decrease in low-power Q_i (to $\sim 200\,000$) upon post-treating the etched resonators in a plasma etch system,[28] for reasons yet to be determined.

In conclusion, we have investigated the effects of interface processing on planar superconducting circuit coherence

at the $Q_i = 10^5$–10^6 level at single-photon powers. At the S-M interface, we showed that contamination from lift-off resist residue and substrate damage from ion bombardment both significantly degrade resonator quality, while substrate roughness had a minimal effect. At the S-V and M-V interfaces, without oxygen treatment we observe post-processing residue that may start to limit planar superconducting qubit coherence at the level of $Q_i \sim$ several million, but find that post-treatment with oxygen plasma can degrade Q_i. It would be worthwhile to systematically test the effect of gentler types of post-ashing techniques on superconducting qubit coherence, about which there have only been anecdotal reports.[43] It would also be important to investigate the influence, if any, of residual films and substrate damage on flux noise and other superconducting qubit dephasing mechanisms.[44,45] Such post-processing studies will likely play an important role in further improving superconducting quantum circuit coherence.

TABLE I. Unexposed resist residue thicknesses of e-beam resist [MicroChem copolymer MMA(8.5)MAA) EL9] and i-line photoresist (Megaposit™ SPR955-CM) on sapphire, Al, and Si, measured by ellipsometry (native oxides are accounted for).

Unexposed resist residue (± 0.3 nm)	Post-strip (nm)	Post-descum (nm)
E-beam resist on sapphire	4.2[a]	0.0[b]
E-beam resist on sapphire	2.5[c]	0.0[b]
E-beam resist on aluminum	2.8[c]	0.1[b]
E-beam resist on silicon	3.9[a]	1.6/0.0[d]
E-beam resist on silicon	0.4[c]	0.0[b]
Photoresist on sapphire	0.2[a]	0.1[b]
Photoresist on silicon	0.1[a]	0.1[b]
Photoresist on aluminum	0.6[a]	0.1[b]

[a]5 min ultrasonic agitation in acetone then isopropyl alcohol (IPA); spin dry.
[b]1 min downstream oxygen ash at 150 °C.
[c]1 h soak in heated N-Methyl-2-pyrrolidone (NMP) ($\sim$70 °C), followed by 5 min ultrasonic agitation in heated NMP then IPA; spin dry.
[d]UV-ozone clean for 10/20 min, respectively.

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