Highly-Multiplexed Superconducting Detector Readout

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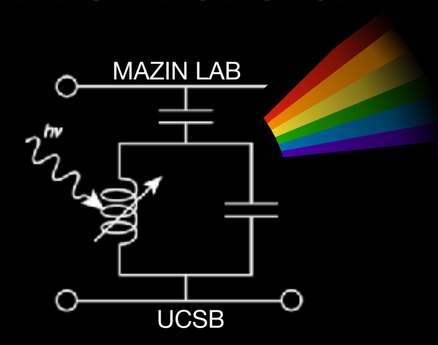


Introduction

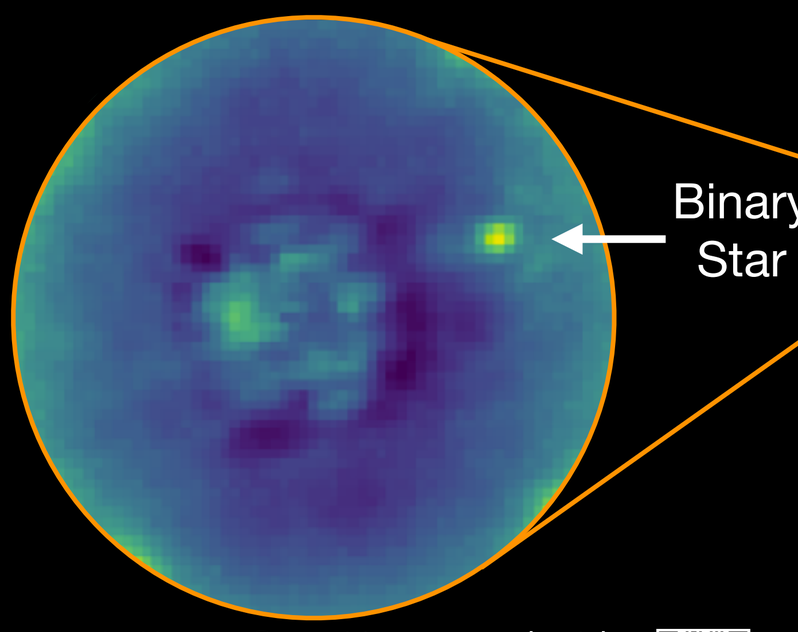
Superconducting Detectors can count single photons with energy resolution across the ultra-violet, optical, and infra-red spectrum with microsecond timing precision.

Allows for advanced image processing techniques using photon statistics to distinguish faint, small features in astronomical observations.

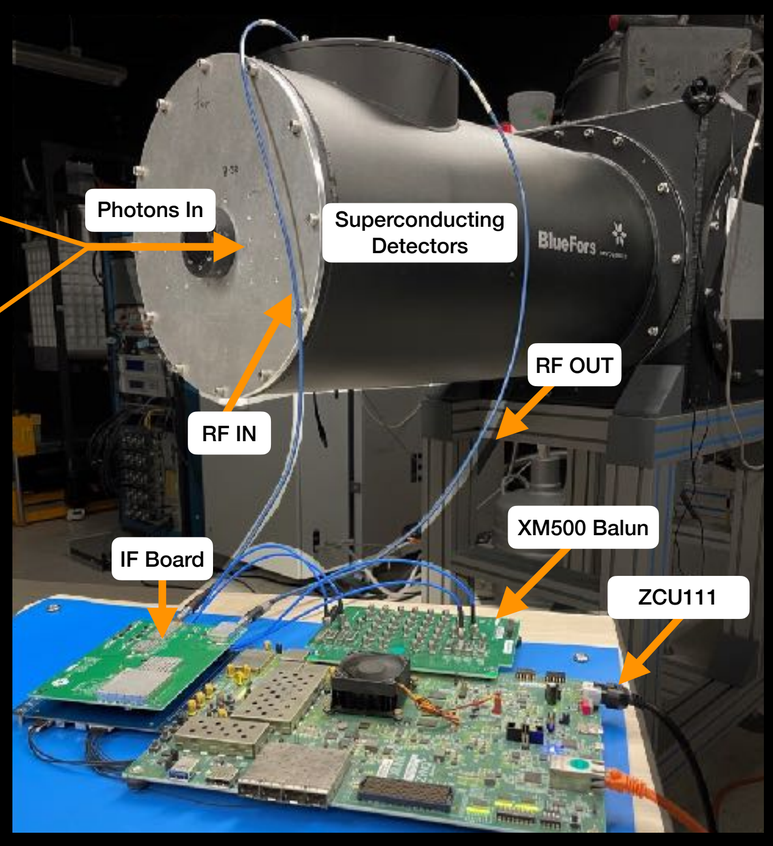
Detectors need to be kept cold with minimal wires to room temperature to be superconducting.

Digital readout must multiplex thousands of readout signals to build megapixel arrays in a single cryogenic system.

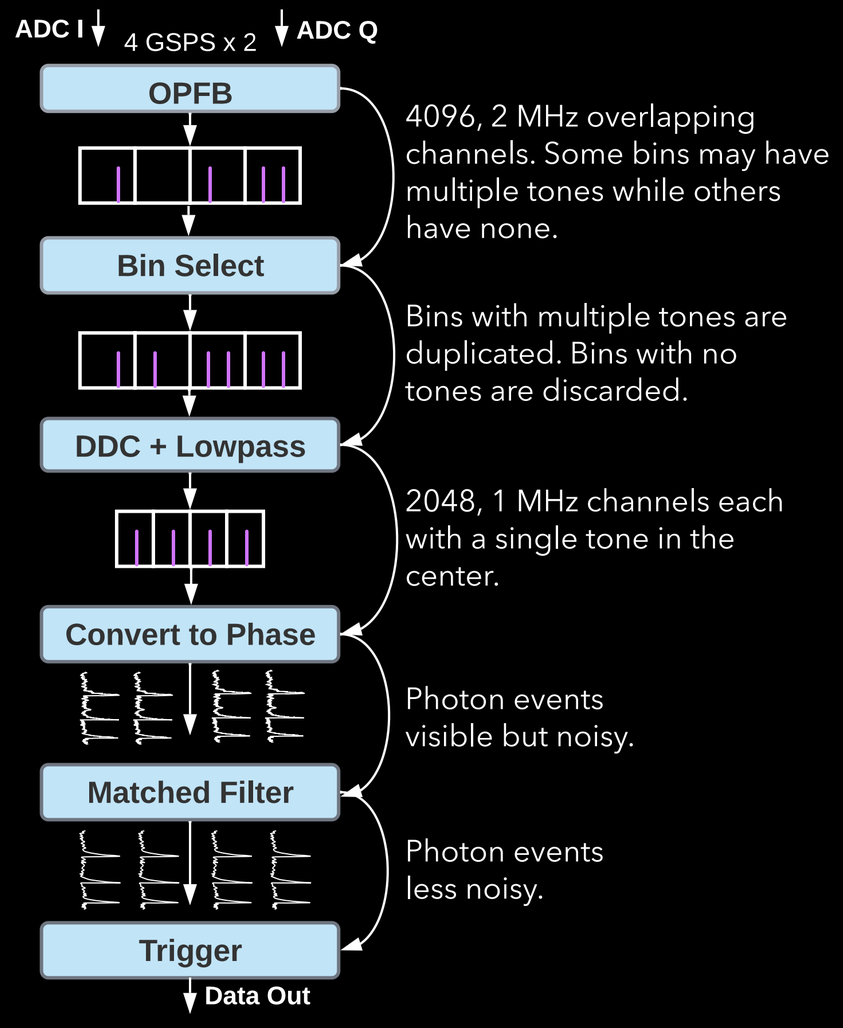
Proposed RFSoC-based system will be able to read out twice as many detectors with one fifth the power and will be easier to use and more maintainable.

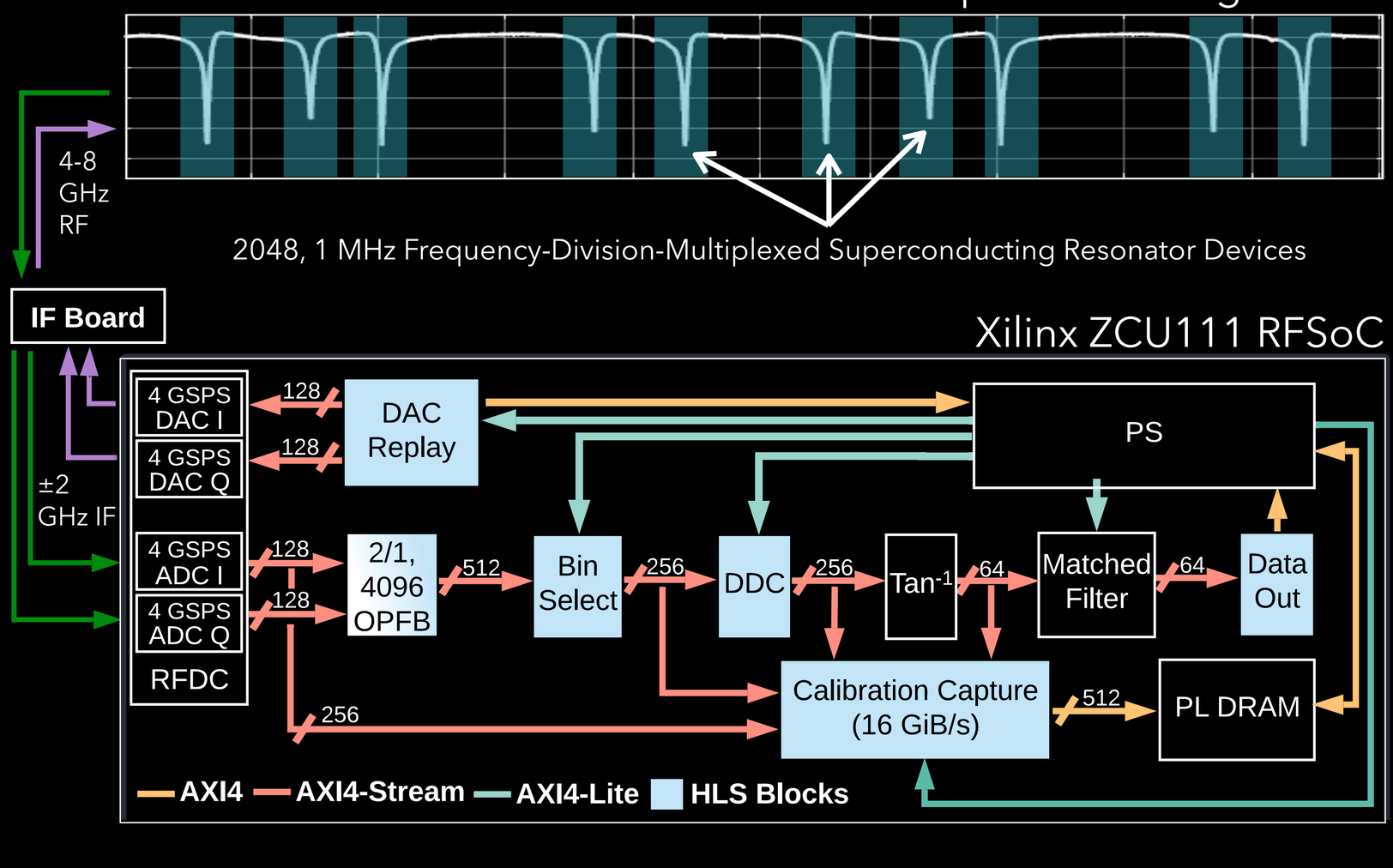


New Binary Star Discovered with Superconducting Detector Array



DSP and Data Flow





Implementation

Vitis High-Level Synthesis

Strategies for High-Performance:

1. Small, single task, HLS blocks are preferable to complex blocks.

2. Clean small internal functions can significantly improve generated HDL.

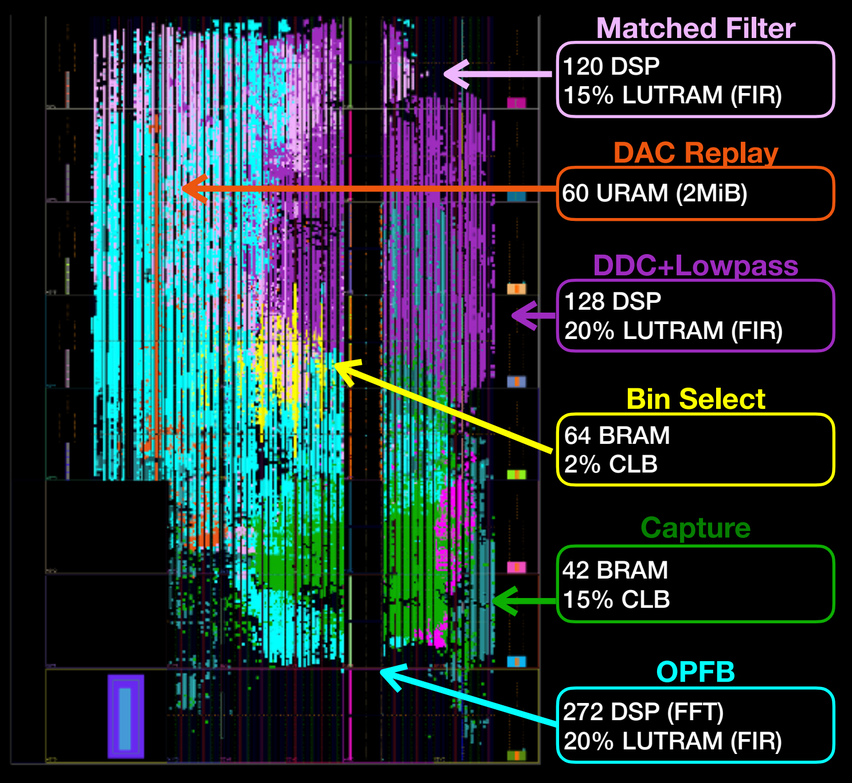
3. Partitioned temporary variables in unrolled loops is preferable to automatic inference within a loop .

4. `ap_ctrl_none` can significantly improve control and logic optimization (by obviating much of it).

5. Manually picking bits instead of `DATAPACK` can be vital.

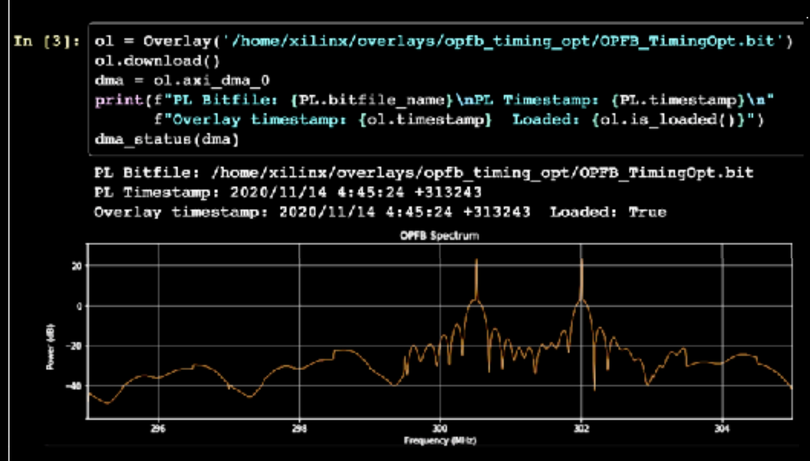
6. External AXIS-AXI is necessary for continuous writes.

Resource Utilization



Verification

Python Productivity for ZYNQ (PYNQ)



```
In [3]: ol = Overlay('/home/xilinx/overlays/opfb_timing_opt/OPFB_TimingOpt.bit')
        ol.download()
        dma = ol.axi_dma_0
        print(f"PL Bitfile: {PL.bitfile_name}\nPL Timestamp: {PL.timestamp}\n"
              f"Overlay timestamp: {ol.timestamp}  Loaded: {ol.is_loaded()}")
        dma_status(dma)

PL Bitfile: /home/xilinx/overlays/opfb_timing_opt/OPFB_TimingOpt.bit
PL Timestamp: 2020/11/14 4:45:24 +313243
Overlay timestamp: 2020/11/14 4:45:24 +313243  Loaded: True
```


Suite of test overlays used to verify individual IP. Python drivers allow simplified interacting with the FPGA through Python.

Github: