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Characterization and Reduction of Capacitive Loss Induced by Sub-Micron Josephson Junction Fabrication in Superconducting Qubits

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Josephson junctions form the essential non-linearity for almost all superconducting qubits. The junction is formed when two superconducting electrodes come within ∼1 nm of each other. Although the capacitance of these electrodes is a small fraction of the total qubit capacitance, the nearby electric fields are more concentrated in dielectric surfaces and can contribute substantially to the total dissipation. We have developed a technique to experimentally investigate the effect of these electrodes on the quality of superconducting devices. We use $\lambda/4$ coplanar waveguide resonators to emulate lumped qubit capacitors. We add a variable number of these electrodes to the capacitive end of these resonators and measure how the additional loss scales with number of electrodes. We then reduce this loss with fabrication techniques that limit the amount of lossy dielectrics. We then apply these techniques to the fabrication of Xmon qubits on a silicon substrate to improve their energy relaxation times by a factor of 5.

Josephson junction (JJ) based superconducting qubits are a promising platform for quantum information processing.[1–4] Based on current performances a powerful and error protected processor will require millions of physical qubits.[4] This number depends strongly on the error rates of individual physical qubits. The ratio of gate operation time to qubit energy relaxation time (T_1) sets a limit on the operation's fidelity. A dominant source of decoherence in superconducting devices is stray coupling to two level states (TLSs) in amorphous dielectrics.[5–8] Strong coupling to TLS defects near their resonant frequency also create 'holes' in tunable qubit spectra which restrict the frequencies available for control operations.[9] Nanofabrication techniques such as photolithography, thin film deposition, and etching tend to leave 1-10 nanometer thick interfacial dielectric films with loss tangents on the order of 10^{-3}, which are difficult to remove.[10] Large strides have been made to reduce the energy loss to these surface dielectrics leading to greatly enhanced T_1's in planar and three dimensional superconducting resonators.[7,11] While qubit T_1's have also improved, they still lag behind those of resonators and appear to be limited by other loss channels.

A key difference between resonator and qubit circuits is the inclusion of JJs. Transmon qubits in particular have two main circuit elements: a linear capacitor and a non-linear inductive element typically constructed from one or more Al/AlO_x/Al JJs. To create capacitors of the highest quality, planar capacitor fabrication can be separated from JJ fabrication and defined identically to planar resonators with critical dimensions of tens of microns.[1,9,12,13] Sub-micron JJs are then shadow evaporated and electrically shorted to the capacitor in a lift-off process. This processing is known to leave behind lossy dielectrics at the surrounding interfaces.[10] Furthermore, electrodes that connect to JJs come within close proximity of each other, concentrating electric fields in nearby interfaces and increasing loss.[14] Thus, a large amount of loss can come from a relatively small amount of lossy material.

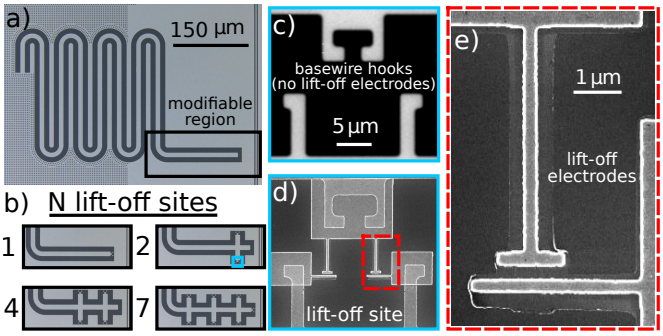

Figure 1. (a) Optical micrograph of a 'hanging' $\lambda/4$ CPW resonator capacitively coupled to a feedline, highlighting the capacitive end we modify to test the loss from different numbers of JJ electrodes. (b) Optical micrographs showing addition of various numbers of lift-off sites modifying the voltage anti-node of the resonator. (c) Zoom in of a single set of basewire 'hooks'. In our standard shadow deposition of JJs we use these hooks to ensure a continuous metal film connects the lift-off JJ electrodes to the basewire metal. (d) SEM image of a single set of basewire hooks with lift-off JJ electrodes attached. (e) SEM image of electrodes showing damaged nearby substrate. Note that there is no dc contact between the two JJ electrodes.

To quantify the additional loss associated with JJ electrodes we mimic the fabrication of JJs connected to high quality coplanar waveguide (CPW) resonators. We add small capacitive 'lift-off sites' to the open end of $\lambda/4$ CPW resonators where there is an electric field anti-node. These lift-off sites emulate the electrodes leading up to but not including the pair of JJs in the superconducting quantum interference device (SQUID) at the base of

Xmon transmon qubits (Fig. 1(c/d)). We measure how loss scales with multiple lift-off sites, effectively amplifying the loss over the background loss of the resonator. We quantify the loss associated with JJ fabrication and use this knowledge to guide improvements in the fabrication leading directly into improvements in Xmon T_1's. The most dramatic improvements occur in Xmons fabricated on silicon substrates, where we see an increase in T_1 by a factor of 5.

We fabricate these resonators with aluminum base wiring on high resistivity (>10 kΩ·cm) intrinsic (100) plane silicon substrates. Prior to loading for deposition, we sonicate bare wafers in acetone then isopropanol and rinse with deionized (DI) water. We then dip the wafers in a heated piranha solution, followed by a DI water, then buffered HF to remove the native oxide. Immediately after blow drying with nitrogen, we load the wafers into a high vacuum electron beam deposition tool and deposit 100 nm of aluminum. We pattern the coplanar wave guide (CPW) resonators, microwave feedline, and launch pads using optical lithography. We develop the resist in AZ 300 MIF (2% TMAH in water) developer. We take advantage of the fact that the developer attacks aluminum to wet etch the pattern in the same step as development.

Next we use electron beam lithography (EBL) to pattern electrodes which mimic JJs'. First, we optically pattern lift-off gold alignment marks, then we pattern and develop the JJ electrode sites using EBL.[9] We then load the wafer back into the same high vacuum deposition tool used for base aluminum. We use an in-situ 400 V, 0.8 mA/cm^2 argon ion mill to etch away the native AlO_x to make DC contact between the etched base wire metal and the lift-off metal.[9,10,15] We immediately deposit aluminum at normal incidence leaving a ∼ 300 nm gap between ground and signal electrodes which mimic the JJ wiring excluding the JJ itself. It is important to note that we do not make DC electrical contact between the resonator's center trace and the ground plane. This gap as well as ion mill redeposited residue is displayed using a scanning electron microscope (SEM) image in Fig. 1(e). A more complete description of fabrication procedures is contained within the supplement.[16]

We show an example of a resonator structure in Fig. 1(a). This resonator is one of ten CPW $\lambda/4$ resonators per chip, each capacitively coupled in parallel to a common feed-line. All resonators are designed with center trace width $w = 24$ μm, gap to the ground plane (g) on either side $g = w$, and resonant frequencies (f_0) between 5.5 and 6.0 GHz. We fabricate CPW resonators with between zero and seven lift-off sites at the voltage anti-node to test the scaling of the additional loss with number of lift-off sites (Fig. 1(b)). The additional lift-off site structures (Fig. 1(b-d)) modify the circuit parameters slightly by adding a parallel capacitance to the open end, but this effect is small (∼1 % of the total resonator capacitance added per lift-off site).[16] We cool these resonators in a heavily filtered[17] adiabatic demagnetization refrigerator with a base temperature of 50 mK and extract their internal quality factor, $Q_i = 2\pi f_0 T_1$ by measuring and fitting the resonators' scattering parameters versus frequency.[7,18] In Fig. 2 we plot this measured Q_i as a function of average photon occupation in the resonator. The low power plateau (around a single average photon occupation) approximates the loss experienced by qubits which also operate at a single photon.

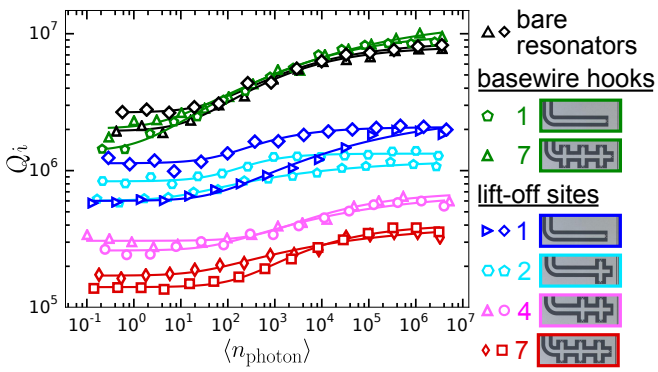

Figure 2. Representative Q_i measurements versus the average number of photons expected in each modified CPW resonator, at a given drive power. These measurements are extracted from S_{21} measurements of the shared feedline near the individual resonances.[7] We fabricate resonators with between zero to seven lift-off sites. While the low power Q_i of resonators with basewire hooks added (one and seven shown) is relatively unaffected, adding lift-off electrodes lowers Q_i dramatically.

The low power Q_i's of the bare resonators (with no lift-off sites) are within the device-to-device variation of bare resonators fabricated separately (between 2 and 3 million). These witnesses indicate that the fabrication process itself has little affect on the quality of bare resonators that are buried by resist during the lift-off processes. Additional base wire 'hooks' are used to connect lift-off to base wire aluminum (Fig. 1(c)). Resonators modified to include these hooks (without performing lift-off) have Q_i near the device-to-device variation of the bare resonators as well, indicating little to no added loss from modifying the base wire in this way. However, when lift-off metal is added, the asymptotic value of Q_i at low photon occupation scales inversely with the number of lift-off sites, and the additional low power loss ($1/Q_i$) per site is 7.9×10^{-7}.[16] This increase of loss with number of JJ electrodes indicates qubits designed with SQUIDs will be twice as sensitive as those designed with single JJs.

The additional loss per lift-off site limits $Q_{i,tot}$ (the total internal quality of the resonator), given by:

$$\frac{1}{Q_{i,tot}} = \frac{1}{Q_0} + \sum_j \frac{p_j}{Q_j}, \qquad (1)$$

where $1/Q_0$ is the background loss from other sources, p_j (the participation) is the ratio of electric field energy

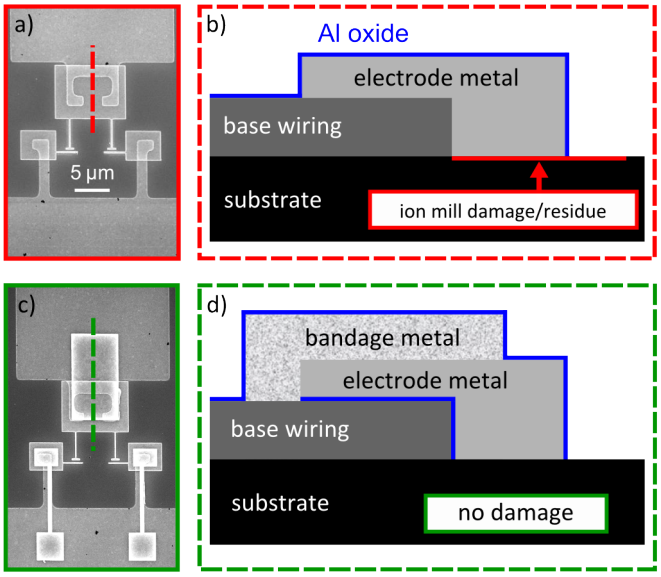

Figure 3. (a/b) SEM image and cross section cartoon of a lift-off site without bandage metal. The substrate is damaged during the argon mill process to remove the native oxide from the base wiring. (c/d) SEM image and cross section cartoon of lift-off site that has undergone the bandage process, making DC electrical contact between electrode metal and base-wiring while protecting the substrate from the ion mill.

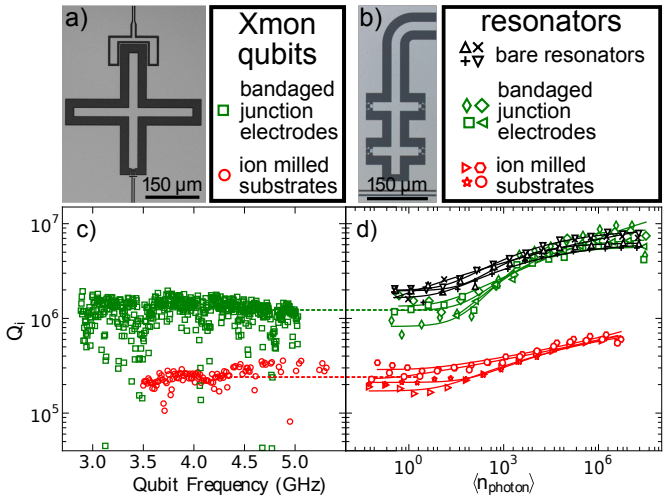

Figure 4. (a) Optical micro-graph of typical Xmon qubit capacitively coupled to readout resonator above, and inductively coupled to SQUID bias line below. (b) Optical micrograph showing capcitive end of a resonator with 4 added lift-off sites. (c) Effective internal quality factor ($2\pi f T_1$) of Xmon qubits fabricated on a silicon substrate with and without the bandage process to protect the nearby substrate during ion milling. Cross capacitor CPW dimensions match the resonators ($w = g = 24$ μm). Horizontal dashed lines show predicted qubit quality by averaging low power Q_i's of lift-off site resonators prepared with the same fabrication method and nearly equivalent participation.[16] (d) Extracted internal quality factor vs average photon number in the resonator. Notice that when the substrate underneath the lift-off metal is not damaged by the aggressive ion mill, the low power internal quality factor is restored to almost that of the bare resonator.

stored in the jth volume to the total capacitive energy and $1/Q_j$ is the dielectric loss of the jth volume. The volume of dielectric between the electrodes is small due to their close proximity, and this small volume may not always contain TLSs sufficiently near resonance to contribute loss.[5] In Fig. 2 we see evidence of this effect when only a single pair of JJ electrodes is added the extracted single photon Q_i varies by over a factor of two between resonators at slightly different frequencies. Adding more sites scales the field energy stored near these electrodes and thus loss due to these interfaces approach a 'loss tangent regime' where Eq. 1 is valid. With enough lift-off sites the total loss of the resonator is dominated by this added loss and will be less dependent on individual TLS fluctuators.

Previous work has shown that aggressive milling of the substrate leads to amorphization and thus added loss at the substrate-metal (SM) and nearby substrate-vacuum (SV) interfaces on sapphire substrates.[10] Using similar experiments on a silicon substrate we found this aggressive ion milled lift-off leaves a roughly 3.9 nm thick interfacial layer underneath the metal. Using cross-sectional finite-element simulations assuming a relative permittivity $\epsilon_r = 11.6$ for this layer we extract an intrinsic TLS loss tangent $1/Q_{\mathrm{TLS}} = \delta_{\mathrm{TLS}} \sim 7 \times 10^{-3}$.[16]

To avoid creating this lossy interfacial layer while still making DC contact to the base wiring we break the electrode deposition into two distinct steps: 'wiring' and 'bandage'. In the wiring step, we use EBL to define the same JJ electrodes as before, but without any in-situ argon mill. We use a downstream oxygen asher to descum the developed resist prior to loading the wafer for deposition. It has been shown that with no in-situ cleaning a descum prior to loading can be used to remove any left over contamination from the development process[19,20] and reduce loss at interfaces.[10] After aluminum deposition we lift-off the resist and unwanted metal in solvents. Second, we use the bandage step to make galvanic contact between the newly deposited lift-off metal and the base wiring. We perform a second round of EBL lift-off, but only expose both metal surfaces (base wiring and JJ electrode). We aggressively ion mill (as detailed above) prior to the bandage deposition. The substrate is protected by resist and the new bandage metal electrically shorts the JJ electrodes to the base wiring (Fig. 3(c/d)). The lithography for the bandage metal can also be done optically and this process has been implemented during the JJ fabrication for Xmon, gmon[21], and fluxmon[6] qubits.

To test the improvement in quality from the bandage process we fabricate resonators with 4 lift-off sites and measure the resulting Q_i's (Fig. 4(c/d)). The low power Q_i's are raised back up to around 1.0×10^6 (a factor of around 5 improvement from the lift-off damaged

sites). A typical Xmon capacitor geometry is shown in Fig. 4(a). In Fig. 4(b) we plot Q_i corresponding to T_1 measurements[16] of qubits that underwent both styles of fabrication. The average Q_i for these qubits is representative of qubits after these processes. The total capacitances of Xmons and the resonators indicate that resonators with 4 lift-off sites have similar lift-off site participation as qubits[16], and the magnitude of improvement is consistent with the average of low power internal quality factor measurements of these resonators (Fig. 4(c)).

Although the bandage process improves Q_i greatly, there still appears to be residual loss caused by the JJ electrodes limiting Q_i below that of the bare resonators, indicating further improvements are possible. There are also sections of the bandaged qubit spectrum where the Q_i drops far below it's average value. These holes occur as the qubits transition frequency (f_{10}) is tuned through the resonance of a particularly strongly coupled TLS.[9] The tunability of the qubit allows for probing loss as a function of frequency while each resonator only probes at a single frequency.

In summary, we modified resonators to use them as a tool to directly measure the added capacitve loss from JJ electrodes necessary for most superconducting qubits. We used this tool to measure different JJ electrode fabrication techniques and found that aggressive ion milling of silicon substrates adds substantial loss. We developed an improved process where we protect the substrate from aggressive ion milling without altering the high coherence capacitor fabrication. We fabricated qubits using this process and measured the average Q_i increase by a factor of 5.

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Supplementary Material for "Characterization and Reduction of Capacitive Loss Induced by Sub-Micron Josephson Junction Fabrication in Superconducting Qubits"

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We provide supplementary data and calculations.

I. LOSS PER SITE WITH AND WITHOUT BANDAGE METAL

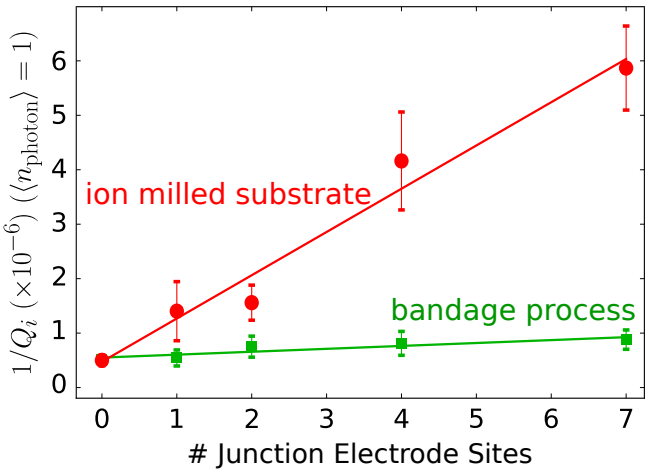

Figure 1. Resonator loss ($1/Q_i$) per electrode site is plotted. Each point and error bar represents the average and standard deviation of at least 4 different resonators on two separate chips. We extract a loss per site (from the line of best fit) for the ion milled substrate lift-off electrodes at a single average photon to be 7.91×10^{-7}, while the same fit for the bandaged process is 5.35×10^{-8}.

Loss at low power scales linearly with the number of Josephson junction (JJ) electrode sites, as shown in Fig. 1. We fit this linear relation to extract the loss per JJ electrode site. We see that the loss is much greater per site for the ion milled substrate process (7.91×10^{-7}) than for the bandaged process (5.35×10^{-8}). Lines of best fit effectively average away effect of device to device variation as well as background resonator Q_i to better extract the loss from a single site. While this experiment stopped at 7 sites, this is an arbitrary upper bound set by design constraints. More sites could be added to amplify the loss further. Plotted points and error bars represent the average and standard deviation of at least 4 different resonators on two separate chips.

II. QUBIT T_1 DATA

Here we plot the measured T_1 data for extracted qubit Q_i plotted in the main paper. We see a stark increase in T_1 in qubits processed using the bandage method. The average T_1 for the bandage junction qubit is 49.4 μs whereas the average for the ion milled substrate qubit is 9.5 μs.

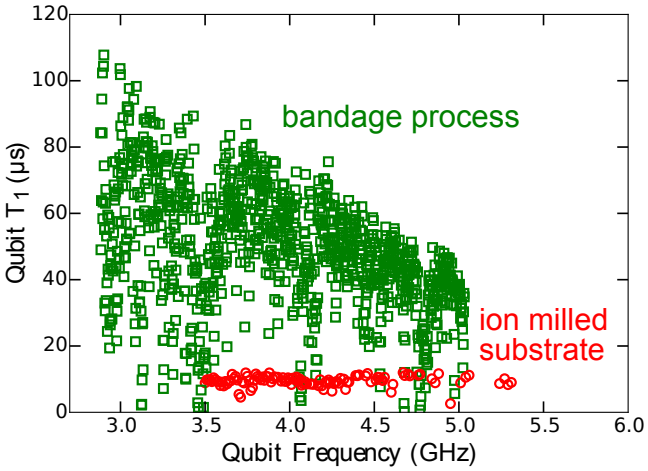

Figure 2. Representative qubit T_1 versus frequency for the two differnt junction processing techniques described in the main paper

III. LIFT-OFF RESONATOR CENTER TRACE EXPERIMENT

We performed an experiment where the entire center trace of the resonator is defined using lift-off, similar to work done before on a sapphire substrate.[1] This experiment isolates the loss from the SM and nearby SV interfaces in a readily simulatable geometry. Basewire preparation was different for these resonators than in the main paper. The bare wafer was prepared in the same way as described in the main paper, but was then loaded into a Ultra High Vacuum ($P_{base} = 6 \times 10^{-10}$ Torr) molecular beam epitaxy system. We heated the wafer in vacuum to

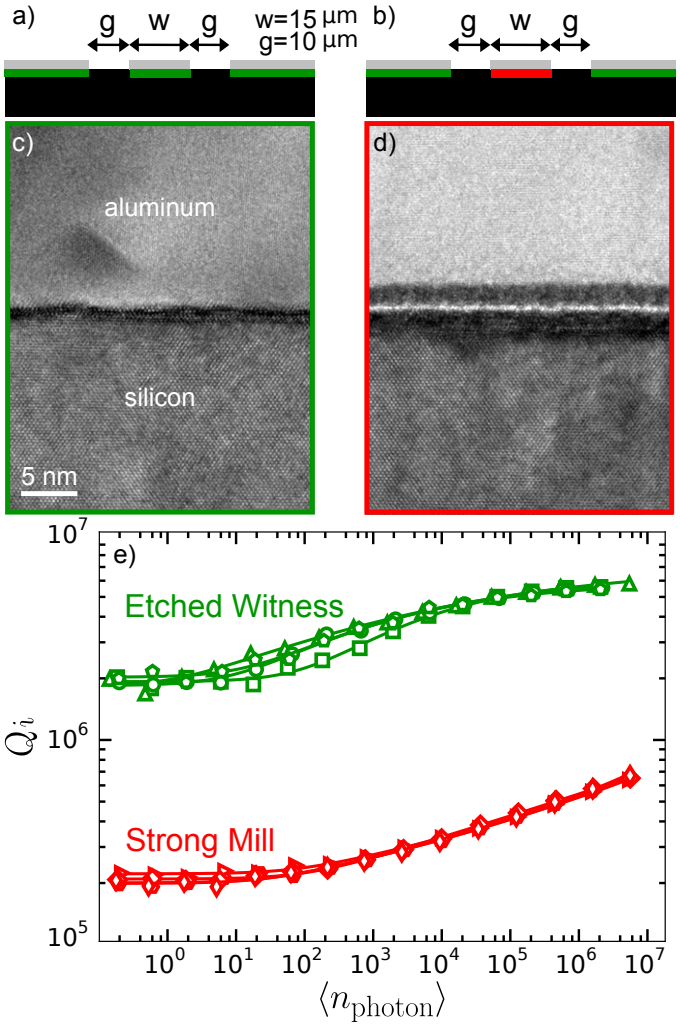

Figure 3. (a/b) Cartoon cross section of resonators where the center trace is defined with etch/lift-off deposited after strong ion mill. The ground plane metal is deposited on HF dipped silicon and defined by dry etch. (c/d) Edge on cross-sectional HRTEM images of the substrate-metal interface under center traces where metal was deposited on HF dipped silicon/lifted off after the strong argon ion mill respectively. (e) Q_i of etched resonator witnesses and resonators where the entire center trace was lifted-off using the junction lift-off process with strong ion mill.

$\sim$ 900 °C and witnessed 2×1 reconstruction. We then allowed the wafer to cool to room temperature in vacuum before depositing 100 nm of Aluminum using an attached electron beam deposition tool. We use photolithography and a dry etch to define the $\lambda/4$ CPW control resonators as well as $w + 2g$ wide holes where lift-off center trace resonators will be formed. Gold alignment marks were then defined using optical lithography and lift-off. We define the center traces for the lift-off resonators using EBL lift-off along with the aggressive ion mill treatment detailed in the main paper.

We display cartoon cross-sections of the etch defined and lift-off defined center trace resonators in Fig. 3(a/b). We show a cross sectional high-resolution transmission electron microscopy (HRTEM) images of the substrate-metal interface of metal deposited on HF dipped silicon and metal deposited after lift-off processing with the strong ion mill in Fig. 3(c/d). We show the internal quality factors of the lift-off center trace resonators and etched witness resonators in Fig. 3(e).

substrate	w (μm)	g (μm)	Q_i (etched)	Q_i (ion milled lift -off center trace)
sapphire	15	10	6×10^5	3×10^5
silicon	15	10	2×10^6	2×10^5

We note a factor of 10 in single photon Q_i between etched and lift-off center trace resonators. We assume the interfacial layer between HF dipped silicon and aluminum in Fig. 3(c) is due to the apparent roughness of the silicon surface $\sim$ 1.6 nm. If we assume this roughness is not changed by ion milling[1], we can estimate the interfacial layer underneath the lifted off center trace (Fig. 3(d)) is 3.9 nm thick. Furthermore, if all excess loss is assumed to come from the SM interface of the center trace, we extract an intrinsic TLS loss tangent $\delta_{\mathrm{TLS}} \sim 7 \times 10^{-3}$ for this layer using 2 dimensional finite-element simulations and assuming a relative permittivity $\epsilon_r = 11.6$.

IV. SIMULATION

Extensive work has been done to simulate participation of interfaces near junction electrodes.[2] We emulate this method to extract expected surface participations for the electrode geometry used in the main paper. We use a finite element solver (COMSOL) to model the electric field density.[3] Whereas a semi-infinite CPW geometry is efficiently modeled in 2 dimensions, a full 3 dimensional treatment is required to understand how the interfaces participate in an arbitrary geometry.[2] We exclude the 1 μm^2 where the actual junction would be be located in simulations. Individual two level fluctuators need to be considered more carefully in such a small volume as the assumptions that lead to a material with a loss tangent become invalid.[4,5]

We apply DC voltage excitation to the center conductor shown in Fig. 4(a) while the ground plane and corresponding lift-off metal was held at 0 volts. We display the circuit diagram in 4(b). The junctions themselves are displayed in black as they are not considered during the simulation. We show a cross-section indicating the different interfaces in 4(c). We calculate the electric field density in the bulk using built-in adaptive meshing. However, to calculate the participations of the three interfaces we apply electro-magnetic boundary conditions as follows:

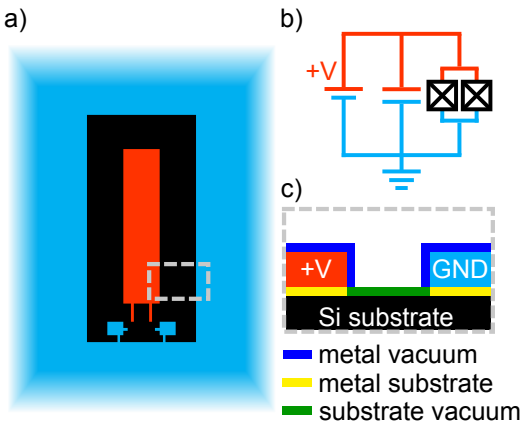

Figure 4. (a) A cartoon representing the 3 dimensional finite element simulation of an Xmon transmon qubit (the length of the CPW section represents the cross capacitor and is adjusted and extrapolated to match the capacitance in a standard design). Where a 1 μm by 1 μm square around the center of where the junction would be located is removed from both signal and ground. (b) A circuit representation of the qubit with applied voltage to measure field distributions in simulation. Junctions are blacked out as they are not simulated. (c) Cross section indicating interfaces of interest.

$$p_j = W^{-1} t_j \epsilon_j \int dA \left|E^2\right| \tag{1}$$

$$p_{mv} W/t_{mv} = (1/\epsilon_{mv}) \int dA \left|E^2_{v,\perp}\right| \tag{2}$$

$$p_{sm} W/t_{sm} = \left(\epsilon_s^2/\epsilon_{sm}\right) \int dA \left|E^2_{s,\perp}\right| \tag{3}$$

$$p_{sv} W/t_{sv} = \epsilon_{sv} \int dA \left|E^2_{v,\parallel}\right| + (1/\epsilon_{sv}) \int dA \left|E^2_{v,\perp}\right| \tag{4}$$

All interfaces are assumed to be the same thickness ($t_{mv} = t_{sm} = t_{sv} = 3$ nm). The metal substrate interface is assumed to have $\epsilon_{r,MS} = 11.6$ (intrinsic silicon), the substrate vacuum interface is assumed to have $\epsilon_{r,SV} = 4.0$ (native silicon oxide) and the metal vacuum interface is assumed to have $\epsilon_{r,MV} = 10.0$ (aluminum oxide). The CPW qubit capacitor was assumed to have $w = g = 24\mu$m and the SQUID wires were assumed to be 500 nm wide. These simulations indicate that around 34% of the energy stored in surfaces in the entire Xmon qubit is stored in surfaces within $\sim$10 μm of the junctions. Combining this knowledge with the increased loss at these interfaces measured in the lift-off resonator center trace experiment, a limit on $Q_{i,tot}$ of the Xmon is set at around 1.4×10^5, which is similar to what we would predict with lift-off site resonator measurements.

V. COMPARING XMON TRANSMON QUBIT AND RESONATOR PARTICIPATIONS OF JUNCTION LEAD SITES

Here we compare how the addition of capacitance through lift-off metal will participate in the trasmon qubit circuit and the resonator circuit. If we have a qubit at 6 GHz with a $w = g = 24$ μm CPW cross capacitor, the length of the capacitor will be roughly:

$$L_{Qc} = 160 \times 4\,\mu\text{m} \tag{5}$$

$$= 640\,\mu\text{m} \tag{6}$$

for a 6 GHz CPW $\lambda/4$ resonator on silicon that is also $w = g = 24$ μm the length will be:

$$L_R \sim 5000\,\mu\text{m} \tag{7}$$

The resonator has a voltage profile extending from the open circuit end to the shorted end of the form:

$$V_{L_R}(x) = V_0 \cos\left[\frac{\pi x}{2L}\right] \tag{8}$$

So, the total energy stored capacitively in the resonator is:

$$E_R = \frac{1}{2}\int C_L V_R^2 dx \tag{9}$$

Now further we assume that there is a constant geometric capacitance per unit length along the whole length of the resonator and so:

$$E_R = \frac{C_L V_R^2}{2}\int_0^{L_R} \cos^2\left[\frac{\pi x}{2L}\right] dx \tag{10}$$

$$= \frac{C_L L_R V_R^2}{4} \tag{11}$$

We neglect the small voltage profile along the length of the capacitor of the qubit due to its extended nature. The total length of the qubit capacitor is only $\sim$ 3% of the wavelength of a 6 GHz oscillation. The capacitive energy stored in the qubit (only considering the cross) is:

$$E_Q = \frac{1}{2}\int C_L V_Q^2 dx = \frac{C_L L_Q V_Q^2}{2} \tag{12}$$

and so if the resonator has on average one photon in it and the qubit has a single excitation in it, the ratio of the voltages will be:

$$E_Q = E_R \tag{13}$$

$$\implies \left(\frac{V_R}{V_Q}\right)^2 = 2\left(\frac{L_Q}{L_R}\right) \tag{14}$$

$$\sim \frac{1}{4} \tag{15}$$

In these calculations we assume that the resonator's capacitance is not greatly effected by our added lift-off sites. We simulate these structures using 2.5 dimensional method of moments software (Sonnet) to justify this assumption. The added capacitance of the lift-off metal is small compared to that of the CPW structures:

geometry	**equivalent lumped capacitance (fF)**
6 GHz CPW $\lambda/4$ resonator	338
typical Xmon cross capacitor	86
typical Josepshon junction (300 nm × 300 nm)	4
CPW stub structure	2.27
lift-off metal	$\sim$ 0.75
basewire hooks	¡0.05

This agrees with SPICE simulations comparing the frequencies of bare resonators and lift-off site resonators. This calculation implies an Xmon qubit will be four times mores sensitive to loss from these junction electrodes than a resonator at the same frequency.

VI. STANDARD FABRICATION

Silicon wafers are 450 μm thick. For base wire and lift-off aluminum depositions we use a Plassys high-vacuum electron beam tool with $P_{base} = 2 \times 10^{-8}$ Torr.

Pre-basewire steps include:

chemical	**time (min)**	**sonicated?**	**temperature**
Acetone	5	Yes	room temp.
IPA	5	Yes	room temp.
Nano-strip (piranha)	10	No	70 C
Buffered HF	1	No	room temp.

In-situ argon ion mill parameters for etching aluminum oxide are:

beam voltage (V)	**beam current density at sample (mA/cm^2)**	**argon flow (sccm)**	**time (min)**
400	0.8	3.6	6

Our photo lithogrpahy process is as follows:

chemical	**spin speed (rpm)**	**post-spin bake temp/time (C/min)**
hexamethyldisilazane (HMDS)	3000	-
i-line resist (SPR 955-0.9)	3000	90/1.5

The nominal thickness of the resist is $\sim$0.9 μm. We use a GCA Auto-Stepper 200 with 0.4 second exposure at $\sim$420 mW/cm^2 at the wafer to expose the resist. We then put the wafer on a 110 C hot plate for 60 seconds to improve resist contrast and development stability. We develop through exposed features in resist after $\sim$60 seconds in developer, but to wet etch, we develop for an additional $\sim$2-3 minutes. The wet etch rate of the aluminum increases greatly as the un-oxidized silicon becomes exposed during the etch. This variable rate leads to aluminum etch back of order 200 nm under the resist and feature rounding. This etch back can be as much as 500 nm on the parts of the wafer that etch through first as the thickness of the metal is non-uniform of $\sim$5-10% across the wafer due to the deposition process. This concentration of TMAH has a strong selectivity toward etching aluminum over the silicon substrate (¿20:1). This selectivity is important as lift-off structures need to "step up" over this etched edge and significant under-cuts would break the circuits. The etch rate of the aluminum is electro-chemically enhanced by the silicon-aluminum interface and can be as much as 10 times faster than the etch rate of aluminum on a sapphire (Al_2O_3) substrate.

We perform lift-off for gold and the junction electrodes as follows. Post deposition we submerge the wafer with resist and lift-off metal in beaker of heated ($\sim$ 80 C) N-Methyl-2-pyrrolidone (NMP) based resist stripper for 1 hour. Once most of the material can be removed with mild agitation we then transplant the wafer into a second heated NMP beaker and sonicate. We remove the NMP by sonicating the wafer in a beaker of isopropynol and then spin the wafer dry at 1500 RPM.

Our electron beam lithogrpahy process is as follows:

chemical	**spin speed (rpm)**	**post-spin bake temp/time (C/min)**
PMMA co-polymer 15% in Ethyl Lactate (MAA)	1500	160/10
Polymethylmethacrylate 4% in Anisole (PMMA)	2000	160/10

The nominal after-bake thickness of the MAA and PMMA are 500 and 300 nm respectively. We then use a JEOL JBX-6300FS EBL system to expose our resist. We e-beam write the full stack using a 100 kV, 2 nA beam, with a 1500 μC/cm^2 dose, while the MAA underlayer is exposed using a 350 μC/cm^2 dose for an expected undercut of the PMMA of around 200 nm. We then develop the pattern in 1:3 Methyl isobutyl ketone (MIBK) to isopropynol for 45 seconds, followed by a rinse in isopropynol for 10 seconds, and blow dry with low pressure (10 psi) nitrogen.

The wafer is heated to a maximum temperature of $\lesssim$150 C for 30 seconds during the descum in the downstream oxygen asher (Gasonics). It is important to note that the e-beam resist is etched during this process ($\sim$50 nm/min) and thus feature sizes are slightly widened. We shrink our design widths to compensate.

VII. MEASUREMENT SETUP

We wirebond the resonator chip into a machined Al sample box with copper pcb inserts. We mount this on the 50 mK cold stage of an adiabatic demagnetization refrigerator. We surround this with a light-tight case which shields from stray thermal radiation from the higher stages which induce extrinsic loss in the superconducting film[6]. We shield the control lines from stray radiation similarly with home-made in-line IR filters at the cold stage.[6] We surround the light tight box with a mu-metal shield to reduce stray magnetic fields (predominantly arising from the superconducting coils used to polarize the salt block to cool the cold stage itself) to a manageable level of $\lesssim$10 mG. We thermalize the control lines at the 4 K stage with 3 in-line 20 dB attenuators, and put the output through a circulator (used as an isolator) to a high electron mobility transitor (HEMT) amplifier both at the 4 K stage. We attach the output of the amplifier to a 3 dB attenuator also at the 4 K stage to reduce standing waves in the line. We perform a through measurement on the feedline near resonance of the individual $\lambda/4$ resonators with a standard microwave vector network analyzer (VNA). For a given power we fit the transmitted wave's amplitude and phase near resonance to an analytic formula for the transmission based on four parameter model for the circuit:

$$\tilde{S}_{21}^{-1}(f) = 1 + \frac{Q_i}{Q_c^*} e^{i\phi} \frac{1}{1 + i2Q_i(f - f_0)/f_0} \tag{16}$$

$\tilde{S}_{21}^{-1}$ is the inverse transmission normalized so far off resonance transmission is 1. The four fit parameters are Q_c^* (the renormalized coupling quality factor of the resonator), ϕ (the phase difference between the small impedance mismatches to the left and right of the resonator on the central feedline), f_0 (the resonance frequency of the resonator), and Q_i (the internal quality factor of the resonator).[7] We then sweep the excitation power of the VNA lower and lower and extract the average photon number inside the resonator based on the excitation power, attenuation, loaded quality factor, and frequency as follows:[8]

$$\langle n_{photon} \rangle = \frac{U}{hf_0} \tag{17}$$

$$\approx \frac{1}{hf_0} \left(\frac{4Z_0}{\pi} \frac{Q_l^2}{Q_c^*} C_L L_R P_{drive} \right) \tag{18}$$

Where U is the internal energy of the resonator, h is Planck's constant, f_0 is the fundamental frequency of the resonator, Z_0 is the characteristic impedance of CPW, $Q_l = 1/Q_i + 1/Q_c^*$ is the loaded quality factor of the resonator, C_L is the CPW capacitance per unit length of the resonator, L_R is the total length of the resonator, and P_{drive} is the power of the traveling wave at the feedline where it couples to the resonator (after all the line attenuations). The single photon limit approximately captures the physics that describes energy loss in superconducting qubits at the same frequency.[7,9]

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