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Qubit compatible superconducting interconnects

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Abstract. We present a fabrication process for fully superconducting interconnects compatible with superconducting qubit technology. These interconnects allow for the 3D integration of quantum circuits without introducing lossy amorphous dielectrics. They are composed of indium bumps several microns tall separated from an aluminum base layer by titanium nitride which serves as a diffusion barrier. We measure the whole structure to be superconducting (transition temperature of 1.1 K), limited by the aluminum. These interconnects have an average critical current of 26.8 mA, and mechanical shear and thermal cycle testing indicate that these devices are mechanically robust. Our process provides a method that reliably yields superconducting interconnects suitable for use with superconducting qubits.

1. Introduction

As superconducting qubit technology grows beyond 1D chains of nearest neighbor coupled qubits [1], arbitrarily sized 2D arrays are a likely next step towards both surface code error correction and more complex high fidelity quantum circuits [2]. While prototypical 2D arrays have been demonstrated [3, 4, 5], the challenge of routing control wiring and readout circuitry has thus far prevented the development of high fidelity 3 x 3 or larger qubit arrays. For example, frequency tunable Xmon transmon qubits on the interior of a 2D array would require capacitive coupling to four nearest neighbor qubits and a readout resonator as well as individual addressability of an XY drive line and an inductively coupled flux line [6]. Routing these control wires with a single layer of base wiring and crossovers is not scalable beyond a few-deep array of

qubits. Multilayer fabrication with embedded routing layers is a natural solution [7], but integrated dielectric layers on a qubit wafer introduce additional decoherence to the qubits [8]. This individual addressability problem can be solved by separating the device into two chips, a dense wiring chip that allows for lossy dielectrics and a pristine qubit chip with only high coherence materials. Combining these two chips to form a hybrid device provides the advantages of both technologies.

A hybrid device is composed of a "base substrate" bonded to a "top chip." Hybridization allows for improved impedance matching between chips as compared to wirebonds and the close integration of incompatible fabrication processes. A qubit hybrid would also benefit from the availability of straightforward capacitive, inductive, or galvanic coupling of electrical signals between the base substrate and top chip through the use of parallel plate capacitors and coupled inductors. Hybrid devices have become ubiquitous in the semiconductor industry, finding applications in everything from cell phones to the Large Hadron Collider [9]. Cryogenic applications are fewer; bolometer arrays for submillimeter astronomy [10, 11] and single flux quantum devices [12, 13] have utilized this technology. Low resistance cryogenic bump bonds [14, 15] and superconducting bump bonds that proximitize normal metals have also been fabricated [16]. Here we present a novel bump bond metal stack up consisting of all superconducting materials with the intent of achieving maximal flexibility in designing flux tunable qubit circuits where mA control currents are necessary.

In order to maintain compatibility with out existing qubit architecture, bump bond interconnects for a superconducting qubit hybrid must meet these requirements:

(i) Bumps must be compatible with qubit fabrication (e.g., aluminum on silicon).

(ii) If interconnects will be used in routing control signals (rather than just as ground plane connections and chip spacers), fabrication yield must be high. e.g., With a 99.9% yield, a device with 1000 interconnects on control lines would yield all lines 50% of the time.

(iii) Interconnects must continue to perform electrically and mechanically after cooling from 300 K to 10 mK.

(iv) Bonding must be accomplished without elevated process temperatures to avoid altering Josephson junction critical currents through annealing [17].

(v) Interconnects must superconduct to provide a lossless connection between chips and avoid local heating.

(vi) The critical current of the interconnects must exceed 5 mA to enable applications in current-biased flux lines.

To satisfy condition (i) above and to extend our wire-routing capabilities through known multi-layer techniques, bumps must provide a connection between aluminum wiring on both the base substrate and top chip. This design consideration will allow us to connect our qubit fabrication to a dense, multi-layer, wire routing device based on standardized CMOS fabrication techniques. Known bump bonding materials that

also superconduct include indium and various soldering alloys. Indium is a natural choice because high purity sources are readily available, it can be deposited in many μm thick layers by thermal evaporation, it has a relatively high critical temperature of 3.4 K, and room temperature indium bump bonding is an industrially proven technology [18]. However, since aluminum and indium form an intermetallic [19], under bump metalization (UBM) it is necessary to act as a diffusion barrier. Fortunately, titanium nitride, fulfills our UBM requirements as it is a well known diffusion barrier (used in CMOS fabrication) with a T_c as high as 5.64 K and has also been shown to be a viable high-coherence qubit material [20, 21].

2. Device fabrication and layout

Figure 1 shows a minimal qubit compatible asymmetric bump bond process used here for DC characterization. The base substrate has a full aluminum/titanium nitride/indium metal stack and, for simplicity, the top chip has just a single layer of indium wiring. In this case, as current flows between the base substrate and top chip, it passes through one aluminum/titanium nitride interface, one titanium nitride/indium interface, and one indium/indium interface. Actual qubit hybrids would be symmetric, with aluminum wiring and titanium nitride UBM on both chips.

For the base substrate, we first blanket deposit 100 nm of aluminum through e-beam evaporation–the same base wiring material used in qubit fabrication [22]. The base wiring, shown in figure (1a), is defined with optical lithography and a $BCl_3 + Cl_2$ plasma dry etch (although lift-off defined aluminum base wiring has been used with similar results). Then, (1b) titanium nitride pads are defined in lift-off resist and the device is placed into a sputter chamber where an *in situ* ion mill (see Appendix C for ion milling parameters) removes the native oxide from the aluminum (1b) before titanium nitride is reactively sputtered in argon and nitrogen partial pressures (1c). After titanium nitride lift-off, the indium pillars are defined in lift-off resist and, then (1d), in a third vacuum chamber, another in situ ion mill (Appendix C) is used to remove oxide and contaminants from the titanium nitride surface, before depositing indium with a thermal evaporator (1e). Also shown in (1e) is the single layer of indium lift off used to define indium wiring on the top chip–this may be done in the same or different indium deposition as the base substrate's indium layer. For the devices we characterized here, we deposited 5 μm of indium on the substrate and 2 μm of indium on the top chip.

After both the base substrate and top chip have been fabricated, an atmospheric plasma surface treatment is used to remove surface oxide and passivate the surface of the indium a few minutes before the two chips are bonded together (1f). This surface treatment is critical to making good indium-to-indium contact during bonding without reflowing the indium [23]. We then flip over the top chip, align the two devices, and compress the dies together using a SET FC-150 flip-chip bonder (1g). Bonding is performed at room temperature with a typical bonding force of 10-20 N per mm^2 of

bump area for 15 μm diameter bumps (2-5 grams/bump), which results in a compression of roughly 40-60% the total height of the two indium depositions. Inspection with an edge gap tool indicates that typically the tilt between the base substrate and top chip is parallel within ± 0.5 mRad, and inspection with an infrared microscope indicates that the xy alignemnt is typically within $\pm 2\,\mu$m.

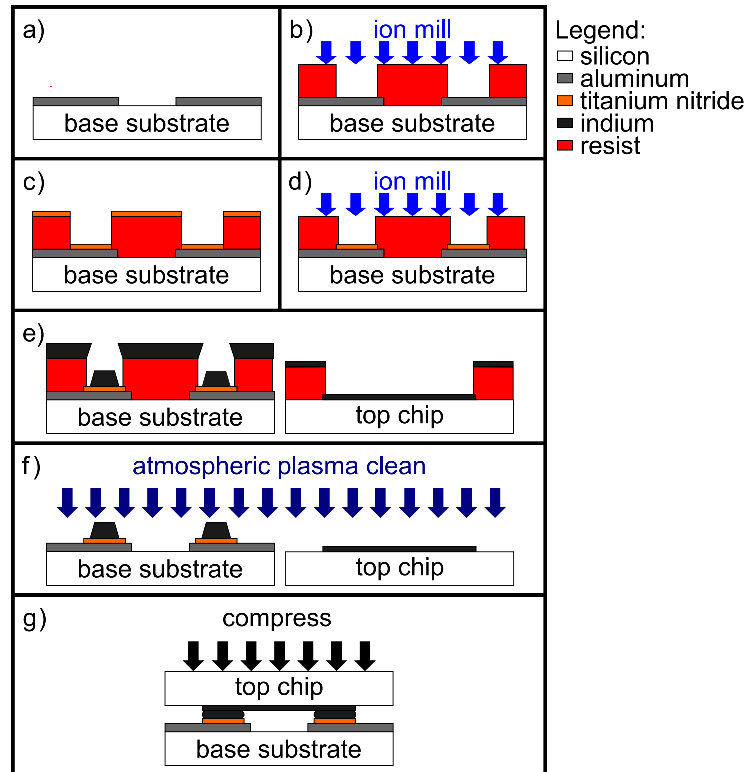

Figure 1. Hybrid fabrication process; (a-d) describe steps specific to the base substrate and (e-g) are common to both the base substrate and top chip. a) On a silicon substrate, a base electrode is defined in 100 nm of e-beam evaporated aluminum by a $BCl_3 + Cl_2$ plasma dry etch. b) The native aluminum oxide is removed by an ion mill at locations defined by lift-off resist. c) In the same vacuum chamber as b), 50-80 nm of titanium nitride is sputter deposited from a pure titanium source in argon and nitrogen partial pressures. d) After lift-off of the titanium nitride and patterning new resist, oxide and contaminants are removed from the titanium nitride by an ion mill at locations defined by lift-off resist. e) In the same vacuum chamber as d), 2-10 μm of indium is deposited by thermal evaporation on both the base substrate and top chip. f) After lift-off of the indium, an atmospheric plasma is used to clean and passivate the surface of both devices a few minutes before bonding. g) The base substrate and top chip are aligned and compressed together at room temperature to complete the hybrid.

Choosing an appropriate bump geometry is subject to several constraints. First, it is desirable to have a chip-to-chip separation of at least several microns so that the impedance of a 2 μm wide, 50 Ω coplanar waveguide transmission line is not dramatically changed by the presence of an overhead ground plane. Providing sufficient separation

allows designs to be insensitive to the final chip-to-chip separation and for a smooth impedance transition as transmission lines travel under the edge of the top chip. In order to achieve a desired separation of 2-10 μm post-compression, 2-10 μm of indium must be deposited on both the base substrate and top chip. When depositing such thick layers of material, especially a high mobility material like indium, sidewall deposition can result in a considerable constriction of the bump feature size. 15 μm diameter bumps were chosen as they have a width to height aspect ratio of 3:2 at the thickest intended bump height; for more information on thick indium deposition see Appendix B. Secondly, the titanium nitride UBM footprint must be large enough so that, after compression, indium does not contact aluminum directly. Given the post-compression alignment accuracy of our flip chip bonder ($\pm 2\,\mu$m) and an expected 50% compression, we find that 30 μm square titanium nitride pads are sufficient for 15 μm diameter indium pillars.

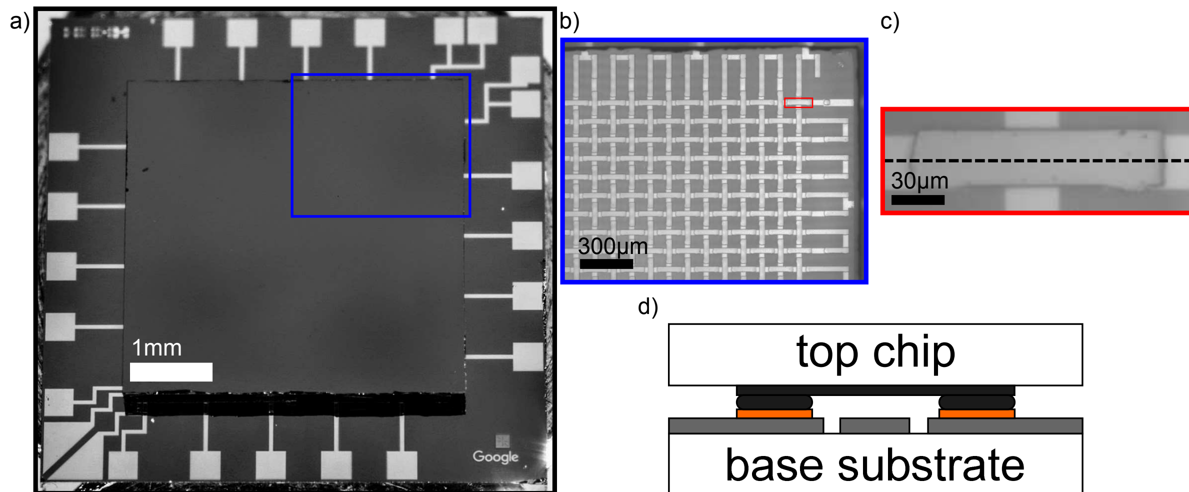

Figure 2. Design of the bump bond DC characterization hybrid. a) Photograph of a hybrid device with a 6 mm x 6 mm base substrate and a 4 mm x 4 mm top chip. b) Infrared micrograph looking through the top chip of the hybrid device. The woven pattern of test circuit can be seen, and bumps are located on either side of the crossings to connect the base wire from the base substrate to the top chip and back. c) Zoomed in infrared micrograph of a a single indium bar on the top chip with interconnects at either end. d) Cross-sectional diagram of the device along the dotted line in c).

The devices characterized here consist of a 6 mm x 6 mm base substrate and a 4 mm x 4 mm top chip shown in Figure 2. In order to electrically characterize a large number of interconnects, we place 1620, 15 μm diameter, circular indium bumps on the base substrate and 30 μm x 150 μm indium bars on the top chip to connect pairs of bumps into a series chain of 1620 chip-to-chip interconnects. At each end of the chain, and every 90 interconnects along the chain, we wire bond to pads on the perimeter of the chip. This wiring configuration allows us to make four-wire resistance measurements by applying an excitation current to any 90 interconnect subsection (or number of subsections of the device) while measuring the voltage across that subsection/s with other leads. Each section of 90 interconnects consists of three rows or columns that extend across the entire

top chip, spread over an area of roughly $2\,\mathrm{mm}^2$. By weaving these rows and columns of together, as shown in figure 2b, we are able to ascertain whether or not electrical failures are spatially correlated. For instance, if one subsection arranged in the rows fails to superconduct or has a suppressed critical current, but none of the columns show the same behavior, it is likely that there are no spatially correlated failures. However, if one section of rows and one section of columns fails, then the intersection indicates a region of interest for failure analysis such as EELS, FIB cross sections, post-shear inspection, or inspection with an optical or infrared microscope.

3. Electrical characterization

We perform low temperature four-wire electrical measurements in an adiabatic demagnetization refrigerator (ADR) down to 50 mK using a lock-in amplifier, ammeter, source measure unit (SMU) and a matrix switch to rapidly characterize a large number of devices. Twisted pair wiring and shielding is used to reduce parasitic coupling between the current excitation leads and voltage sense leads. Common mode voltage correction is implemented with the matrix switch which also allows us to quickly switch between measurements. For a detailed look at the measurement system as well as the the resistance and critical current measurements discussed below, see Appendix A.

This setup allows us to make a resistance measurement of the device in its superconducting state. Using common mode compensation and the lock-in amplifier with a several mA sinusoidal test current, we are typically able to bound the resistance of a series chain of 1620 interconnects to be less than $5\,\mu\Omega$ below 1.1 K, which is an average resistance of $3\,\mathrm{n}\Omega$ per interconnect. Figure 3a shows a typical resistance versus temperature curve for a full 1620 interconnect chain and a 2 interconnect test structure on the same device. At 1.1 K we observe a clear transition to a superconducting state when the resistance of 1620 interconnects in series falls more than 7 orders of magnitude to a few $\mu\Omega$. The resistance measured below 1.1 K is roughly the same for both 1620 interconnects and the 2 interconnect test structure which indicates that this measurement is likely limited by system parasitics or measurement electronics rather than by an actual resistance or the inductance of the device. In figure 3b we use a SMU to assess the critical current of each of the eighteen 90 interconnect subsections on three hybrid devices. The average critical current for each subsection is 26.8 mA, with a number of subsections above 30 mA and a single subsection with a suppressed critical current of 10.3 mA. This data represents 4860 interconnects, 100% of which superconduct with a critical current above 10 mA. Furthermore, at least 98% of the interconnects have a critical current above 24.5 mA. Since there was only one section of rows (and no columns) with a suppressed critical current, it is likely that a single interconnect could be responsible for the lower critical current. The high yield of this process and lack of spatially correlated failures indicate that parallel interconnects can be used to further increase the critical current and/or to serve as precautionary redundant connections (though we yielded 100% on these 3 test devices and have had similar yields

across several generations of test devices). The average room temperature resistance of these 90 interconnect subsections is 47.7 Ω with a standard deviation of 2 Ω indicating reasonable bump uniformity. Typically we find that a room temperature resistance <1 Ω/interconnect (including the aluminum and indium base wiring used to chain them together) indicates that the flip chip bonding was successful. We find that insufficient compression or a bad material interface results in a resistance higher than 1 Ω per interconnect.

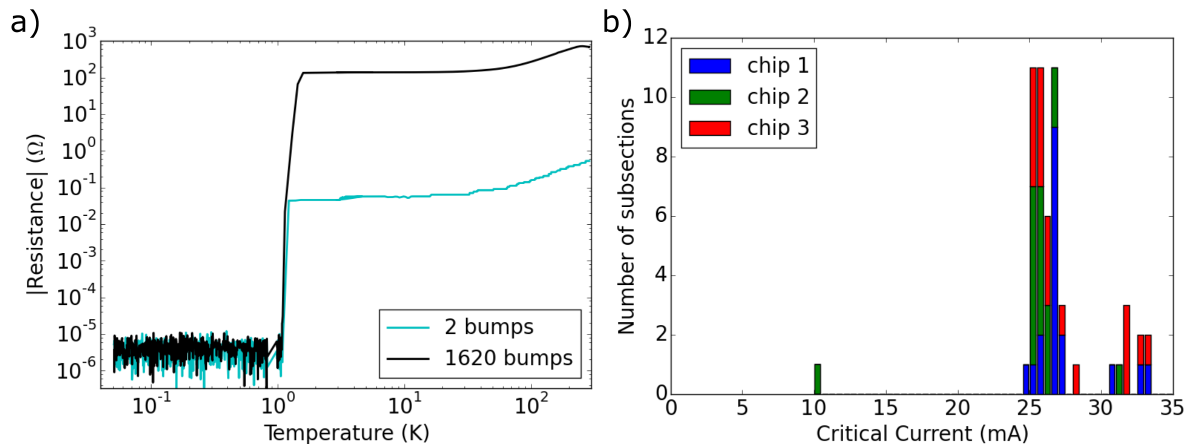

Figure 3. Electrical device characterization. a) Typical four-wire resistance measurement versus temperature for a chain of 1620 interconnects and a 2 interconnect test structure on the same device from room temperature to 50 mK. A superconducting transition can be seen at 1.1 K where the resistance of both the 1620 and 2 interconnect structures fall to a few $\mu\Omega$. For the 1620 long chain, this measurement demonstrates a superconducting resistance more than 7 orders of magnitude lower than its normal state resistance at 3 K. b) Histogram of critical currents for each of the eighteen 90-interconnect subsections on three different chips. The average critical current is 26.8 mA with >98% of the subsections above 24.5 mA

4. Mechanical characterization

Several mechanical tests were performed on a different generation of hybrids consisting of a 10 mm x 10 mm substrate and a 6 mm x 6 mm square chip. These devices had about four thousand 20 μm diameter circular bump bonds spread fairly evenly over the 36 mm^2 area of the top chip. In order to characterize the mechanical strength of these interconnects, destructive shear tests were performed in which a force is applied to the edge of the top chip, parallel to the face of the chip (e.g., force was applied in the plane of the page as the chip is shown in figure 2a), until the top chip separates from the substrate. Four devices were tested; three separated at 35 N and one exceeded the limits of the tool at 49.9 N, all of which are more than sufficient to ensure that devices are robust enough for handling. Finally, thermal cycling was performed on a device that had been previously confirmed to be fully superconducting below 1.1 K. One hundred thermal cycles from

-80 °C to 45 °C were performed with a 23 minute dwell at both -80 °C and 45 °C and a 20 °C/min ramp rate for transitions. After 100 thermal cycles (and unknown conditions during round-trip ground shipping to our off-site lab) the sample was cooled back down to 50 mK. All interconnects on the device still remained superconducting, although with a suppressed critical current of 1-5 mA in most subsections down from 20-25 mA in the initial characterization of this device. It is also worth noting that the devices measured in figure 3 were cycled from room temperature to 50 mK and back as many as three times in our ADR (approximately 0.2°C/min average warming/cooling rate) with no measurable impact on the critical current.

5. Conclusion

The flip chip hybrid devices we have developed offer a viable solution to control signal routing in two-dimensional high-coherence circuits. These interconnects, consisting of a titanium nitride diffusion barrier and indium bumps, serve as electrical interconnects between two planar devices with aluminum wiring. This fabrication process opens the door to the possibility of the close integration of two superconducting circuits with each other or, as would be desirable in the case of superconducting qubits, the close integration of one high-coherence qubit device with a dense, multi-layer, signal-routing device. Furthermore, these interconnects have a typical critical current above 25 mA which is an order of magnitude larger than the largest typical DC control currents used to flux-tune superconducting qubits. Limited by the aluminum, these bumps are fully superconducting below 1.1 K, and below this critical temperature, we are able to estimate the resistance of each bump to $< 3\,\mathrm{n\Omega}$. These high yield, mechanically robust, and high critical current electrical interconnects are ready to be implemented into more complex circuits including 2D arrays of nearest neighbor coupled flux-tunable superconducting qubits.

Acknowledgments

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Appendix A. Electrical characterization measurement setup

Accurately bounding the resistance of a suspected superconducting device requires the ability to very accurately measure the excitation current and the resulting voltage drop across the device, which should be zero. Even when care is taken to use appropriate wiring and grounding, as shown and described in Figure A1, DC based measurements are subject to thermoelectric voltages, broadband noise, and measurement ranges optimized for non-zero resistance materials where finite voltages are expected. We use an AC excitation and a digital lock-in amplifier to mitigate these effects, but the resulting measurement is not without difficulties. A lock-in amplifier implements mixing and filtering to extract the signal amplitudes both in phase and 90-degrees out of phase with a reference tone at the specific reference frequency. By using the sinusoidal excitation as the lock-in amplifier reference, we are able to measure the voltage across our device and extract the in phase voltage (V_x) and quadrature voltage (V_y) across our device.

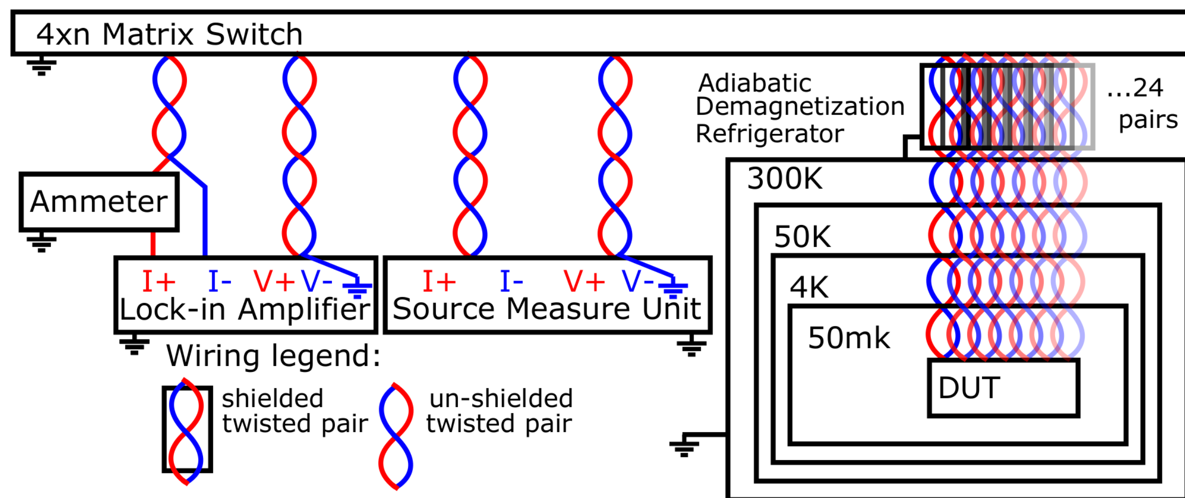

Figure A1. Schematic of our measurement setup. A 4 by n matrix switch is used to route two sense and two excitation lines from various measurement equipment, including a lock-in amplifier and a source measure unit, to our bump bond devices. Both the measurement equipment and DUT are connected to columns of the matrix switch and the rows are used to connect any column to any other column. The measurement equipment chassis are all grounded to a common surge protector. The twisted pair shielding is grounded at the ADR, and floating at the matrix switch. The four-wire measurement ground is provided by the negative excitation terminal of either lock-in amplifier of SMU.

Figure A2 shows a model of the 4-wire measurement circuit used to perform our bounding resistance measurement. The voltage excitation signal is provided by an adjustable frequency sine-wave generator with a $50\,\Omega$ output impedance. An ACrms ammeter is placed in-line with the positive voltage lead of the sine-wave generator to measure the excitation current, which is set by the amplitude of voltage waveform and the approximately $50\,\Omega$ lead resistance in the I_+ and I_- leads. This lead resistance is

dominated by the NbTi wiring used in our cryostat all the way from 300 K to the 50 mK stage and varies by 10-20% channel-to-channel. This lead resistance variation is why we measure the excitation current directly with the ammeter rather than inferring it from the excitation voltage.

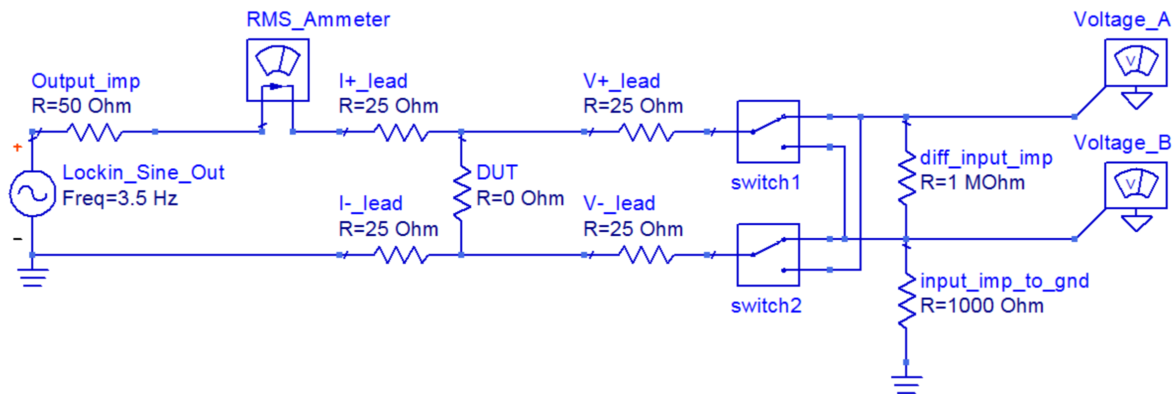

Figure A2. A model of the 4-wire measurement circuit used to perform our bounding resistance measurement.

It is important to note that this wiring configuration results in a common-mode voltage at the sample approximately equal to half of the excitation voltage due to the voltage divider created by the excitation leads. Our lock-in amplifier has a common mode rejection ratio (CMRR) of 100 dB meaning that common mode (CM) voltages may leak into the differential voltage measurement attenuated by 10^5. Without further common mode compensation (and independent of the excitation voltage) the 50 Ω lead resistance and CMRR specification would limit our measurement accuracy as follows. The excitation current is approximately equal to the excitation voltage divided by the total of the voltage source output impedance and the sum of the two excitation leads:

$$\mathrm{I_{ex}} = \mathrm{V_{ex}}/\mathrm{R_{lead+source}} \tag{A.1}$$

Since the excitation leads are approximately equal, the common mode voltage on both sense leads will be approximately $V_{ex}/2$ and the lock-in amplifiers CMRR specifies how much of this voltage may leak into its differential voltage measurement:

$$\mathrm{V_{cmleakage}} = \mathrm{V_{cm}} * \mathrm{CMRR} = \frac{\mathrm{V_{ex}}}{2} * \mathrm{CMRR} = \mathrm{V_{ex}} * 5 * 10^{-4} \tag{A.2}$$

Combining A.1 and A.2 we find that the common mode leakage and lead resistance would limit our measurement to a minimum of 500 $\mu\Omega$.

$$\mathrm{R_{min}} = \frac{\mathrm{V_{cmleakage}}}{\mathrm{I_{ex}}} = \frac{\mathrm{V_{ex}}}{2} * \mathrm{CMRR} * (\frac{\mathrm{V_{ex}}}{\mathrm{R_{leads+source}}})^{-1} = 500\,\mu\Omega \tag{A.3}$$

Compensation for this common mode voltage leakage is accomplished by taking two voltages measurement using the switches shown in figure A2. While holding the excitation signal constant, the switches are used to reverse the polarity of the voltage sense leads and two measurements are recorded:

(i) Differential Voltage_A-Voltage_B + common mode leakage, and

(ii) - Differential Voltage_A-Voltage_B + common mode leakage

The sum of these two measurements give us two times the common mode leakage and the difference gives us two times the differential voltage of interest. Figure A3 shows these two voltage measurements as well as the computed common mode (CM) and differential voltages for the V_x and V_y signals measured across a 1620 bump structure. From this data we can confirm that the lock-in amplifier is meeting its common mode rejection specification of >100 dB, as well as its input noise specification of $6\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$. Since we are using a 0.3 s time-constant we expect and confirm the noise we see is <˜11 nVrms.

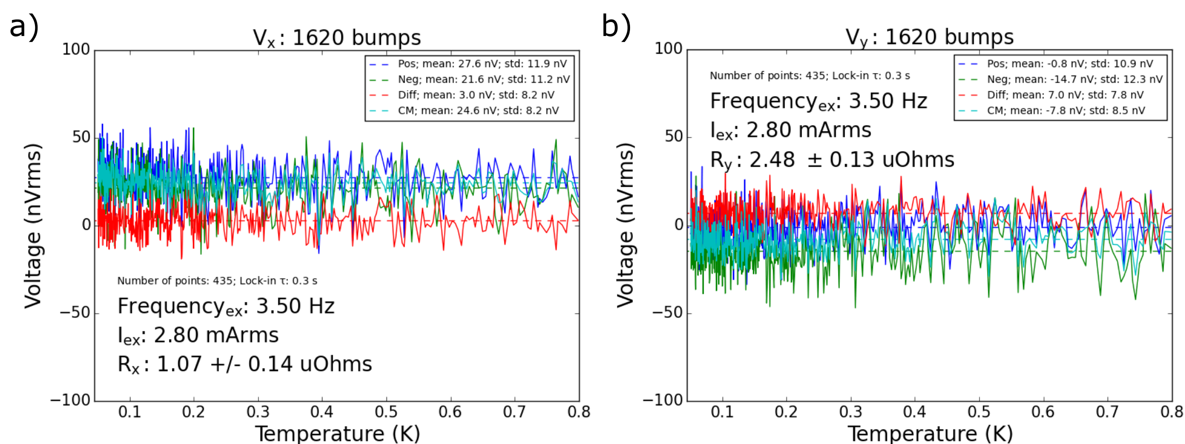

Figure A3. Typical Vx and Vy voltages traces with positive and negative lead polarity. The differential voltage computed from the difference of the positive and negative polarity measurements is near zero and the common mode voltage computed from the sum is consistent with the lock-in amplifiers CMRR specification of 100dB (we usually see 110-140 dB).

Since the lock-in amplifier is making an AC measurement, care must be taken to make sure inductances and capacitances do not affect the measurement. Firstly, it is very important to use twisted pair wiring for at least one pair of, and preferably both, the sense +/- leads and the excitation +/- leads (and preferably shielding where possible to further reduce mutual inductances of the sense and excitation leads and to further reduce electromagnetic noise pick up). By utilizing twisted pairs in this configuration, the mutual inductance between these leads is reduced considerably–without twisted pairs, one easily ends up with a several μH or more mutual inductance between the sense and excitation leads which will end up looking like an in-phase voltage (or real resistance). Secondly, the voltage signal from the inductance of the sample as well as other parasitic inductors and capacitors should be proportional to the frequency of our excitation voltage–to reduce the impact of such signals and parasitics, we work at very low frequencies, typically $< 10\,\mathrm{Hz}$. Finally, we typically find that the resulting differential voltage is proportional to both the excitation voltage as well as the excitation frequency indicating that the signal we are measuring is due to a system parasitic and is

not just electronics noise. The frequency dependence in particular hints that this load is primarily not resistive, but even if we take the conservative approach of assuming it is all resistive, we are able to limit the resistance of a series chain of 1620 bumps to be several $\mu\Omega$. The fact that the differential voltage measured across 1620 bumps is basically the same as for 2 bumps is further evidence that the measurement is dominated by a cabling parasitic and not an actual resistance on our sample, or even the samples inductance.

Measuring the critical current of our devices in an Adiabatic Demagnetization Refrigerator (ADR) required some optimization. An ADR uses a helium compressor to cool a superconducting magnet and sample stage down to 3-4 K. Then, to cool the sample down to 50 mK, you perform a magnet cycle where the superconducting magnet is used to align magnetic dipoles in a salt crystal. After a 30-45 minute soak time in this magnetic field, the salt crystal and sample stage are thermally disconnected from the rest of the system and the magnetic field from the superconducting magnet is ramped down. When the magnetic field approaches zero, the dipoles in the salt crystal begin to mis-align, pulling heat out of the system. That is all to say, an ADR is a single-shot cryostat with a cycle time of about 90 minutes if you heat up the sample too much and need to cool back down. These devices have a critical current > 25 mA, and once we drive a subsection normal by exceeding the critical current, the sample stage of the cryostat heats up from 50 mK to 3 K in a about a second if the current is not reduced. In order to efficiently characterize many devices, care had to be taken to avoid unnecessarily heating the cryostat.

In order to limit the heat dissipation in our sample, we used a source measure unit (SMU). A SMU is a combination source (with a configurable current or voltage set point) integrated with a meter (configurable for current and/or voltage). In our use case, we just apply current and measure the voltage across our sample–as we increase the current, if the voltage across the sample jumps above the noise level, then we know the sample went normal. SMUs are fast, accurate, and offer a number of very nice features that ultimately allowed us to make hundreds of critical current measurements in a single magnet cycle. Firstly, our SMU offers pulsed operation where the source provides a timed current pulse of a few ms and the measurement aperture is synchronized to occur just after the excitation has settled. We found that we were able to achieve good results using just a 2 ms long current pulse. Furthermore, our SMU offers a voltage protection feature where the source terminals are physically disconnected inside the unit with a relay if the source compliance condition (compliance voltage in our case) is reached. Since we are measuring a superconducting material, the compliance voltage at our device should be 0 V, so we set a limit at 5 mV and found that these results were in good agreement with measurement where we did not pulse the excitation.

Appendix B. Material and interface characterization

Aluminum is deposited using e-beam evaporation in a vacuum chamber with a base pressure of 1e-7 mBar. 100 nm of aluminum is deposited at a rate of 1 nm/s. Structures were patterned and etched using standard lithographic techniques and $BCl_3 + Cl_2$ chemistry in an inductively coupled plasma etcher. (Other samples have yielded using both wet etches and lift-off defined structures.)

The titanium nitride under bump metalization (UBM) is used as a diffusion barrier between indium and aluminum as both are known to be very reactive metals [19]. To achieve a dense film with low oxidation and Tc above 3 K, we employ a substrate bias during deposition [24]. A 50-80 nm titanium nitride film is grown using a reactive sputter (150 W power) from a pure titanium target in 3 mTorr of argon and nitrogen (48 sccm and 1.75 sccm flows, respectively).

The resulting films are found to be nearly stoichiometric, but slightly nitrogen rich using XPS (Figure B1) and RBS (Table B1). Moreover interdiffusion of aluminum into the titanium nitride is absent.

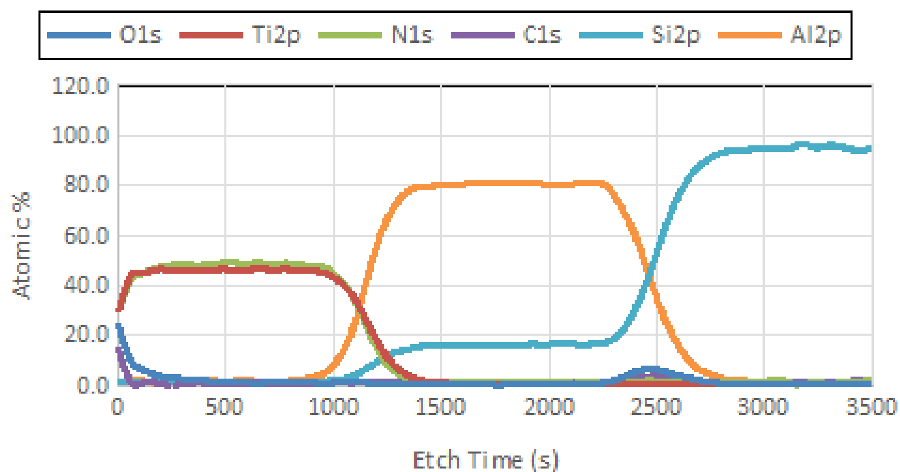

Figure B1. XPS data for a layer of titanium nitride on aluminum on a silicon substrate.

Table B1. RBS data for a 320 Å titanium nitride layer on 1000 Å on a silicon substrate.

	"RBS" Thickness [Å]	Atomic Concentration [at%]						Assumed Density [at/cc]
		N	**Si**	**Ti**	**Al**	**W**	**Ar**	
Layer 1	320	53.5	-	46.5	-	-	-	1.07E23
Layer 2	10	-	-	-	29.7	3.7	66.6	3.79E22
Layer 3	1000	-	-	-	100	-	-	6.02E22
Bulk	-	-	100	-	-	-	-	.5.00E22

Since titanium nitride is employed as a diffusion barrier, it is deposited as square pads beneath the indium bumps. These pads are defined in lift-off, using a single layer of positive photoresist and a MIB (AZ Developer) developer to prevent etching and roughening of the underlying aluminum during developer rinse. To make good electrical contact between the titanium nitride and the underlying aluminum, the patterned aluminum wafer is ion milled in-situ before sputter deposition. Mill parameters are shown in Appendix C (120 s mill time).

After the titanium nitride is lifted off, the wafer is patterned again using a lift-off polarity and a thick positive resist. Circular apertures are opened using a MIF developer (since the aluminum is encapsulated by corrosion resistant titanium nitride). The wafer is loaded into a thermal evaporator with a base pressure below 1E-7 Torr. To remove any contaminants and insulating oxides, the wafer is ion milled *in situ*, then allowed to cool on the water cooled chuck (held at 0 C). Indium is deposited at rates exceeding 2 nm/s to prevent a constriction of the lithographically defined apertures by crystallite growth. Figure B2 is a SEM of typical crystallite growth that occurs when slow deposition rates are used. Indium lift-off is performed in a heated NMP bath.

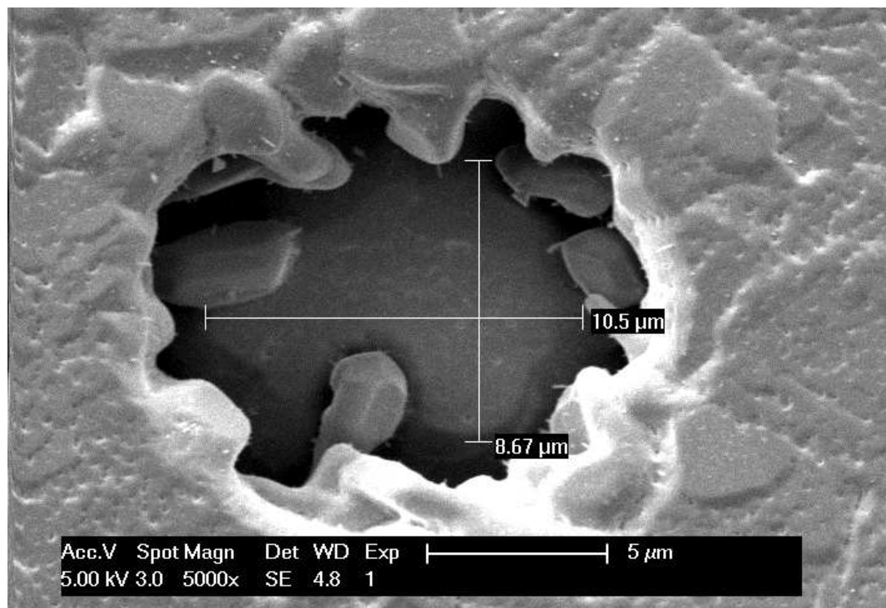

Figure B2. SEM image of indium crystallite growth over a 15 μm diameter hole during a slow (<1 nm/sec) indium deposition.

The entire material stack up has been characterized using FIB cross sections and EELS spectroscopy to determine the composition of the layers and, most importantly, their interfaces. Crucially, no indium-aluminum interdiffusion exists across the titanium nitride barrier. However, intermittent oxide contamination (up to 15% by atomic percent) at the titanium nitride/indium interface and titanium nitride/aluminum interface has been measured on various samples, although this seems to have little effect on yield or critical current.

Appendix C. Ion mill parameters

Table C1. *in situ* ion mill parameters used to clean aluminum surface before depositing titanium nitride.

	Cathode	Discharge	Beam	Accelerator	Neutralizer	Emission
Voltage (V)	7.3	40.0	399	79	18.9	n/a
Current (A)	10.8	0.48	0.055	0.0031	17.2	0.118

Table C2. *in situ* ion mill parameters used to clean titanium nitride surface before depositing indium.

	Cathode	Discharge	Beam	Accelerator	Neutralizer	Emission
Voltage (V)	9.3	40.0	600	120	10.4	n/a
Current (A)	14.9	1.52	0.12	0.004	0.0122	0.116