Lab #1: Quartus test drive

Physics 127BL Winter 2024

Lab report due **Friday, January 19, at 11:55 P.M.**

Please read the lab report and homework guidelines handout on the course web page.

Introduction

This week in lab and lecture we will discuss elementary logic gates. The lab exercise described here will help you learn how to enter gates into Quartus, wire them together, and simulate their function. You will practice using Quartus and solve a few simple combinational logic problems in preparation for configuring a field programmable gate array (FPGA).

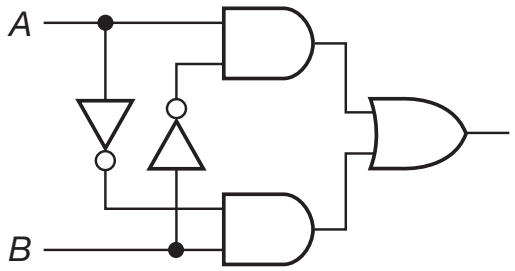
Exercises

For each circuit listed below, compute the truth table. Enter the circuit into Quartus, then design and run a functional simulation that covers all possible input states. Verify your truth table using the simulation output.

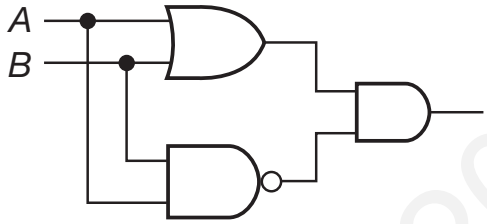
In your lab report, include the truth table and a screen shot of the simulation output window for each circuit. For circuits with more than one gate, include a screen shot of the circuit diagram in Quartus.

1. An inverter, also known as a `NOT` gate.
2. An `AND` gate.
3. An `OR` gate.
4. A `NAND` gate.
5. An `OR` gate built only of `NAND` gates (design this).

6. This circuit:



7. This circuit:



   This is known as an "exclusive `OR`" (`XOR`) circuit.

8. A circuit with inputs labeled "is raining," "am outside,", and "have umbrella," with output "stay dry" that implements the following sentence: "If it is raining and I am outside with no umbrella, I will get wet."